Reference AG

PIXELWORKS PRODUCTS

TECHNOLOGY

Our designs are based on self-contained modules that can be reassembled and reused in new development programs. We extensively simulate and test our designs using the best available simulation and synthesis tools and internally developed proprietary validation tools. We work closely with our foundry partners to use state-of-the-art deep-submicron process technology.

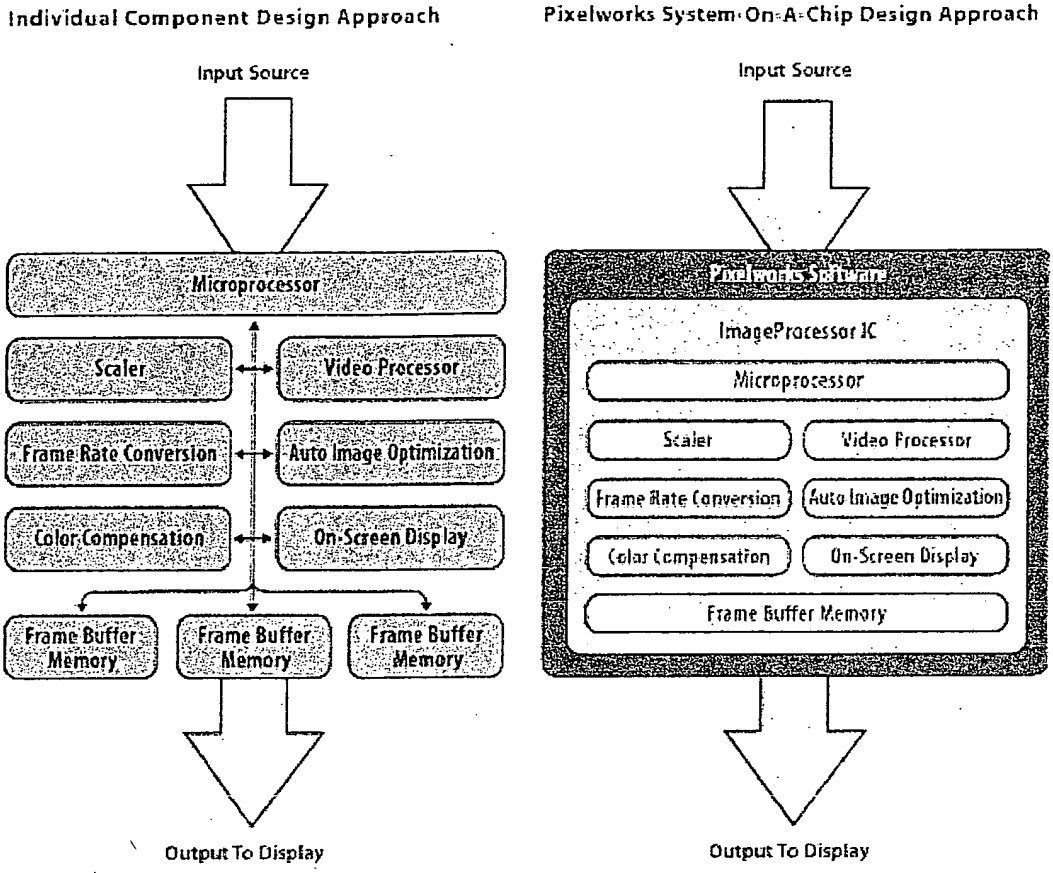
We have used this design methodology to produce first-turn silicon success, as demonstrated in our development of what we believe to be the world's first 0.25 micron system-level integration application-specific ICs with embedded DRAM.

IMAGEPROCESSOR IC TECHNOLOGY

UNIQUE ON-CHIP INTEGRATION OF MICROPROCESSOR, MEMORY AND DIGITAL SIGNAL PROCESSOR. Our system-on-a-chip architecture features an embedded x86-compatible microprocessor and peripherals, 4 megabytes of ultra high bandwidth DRAM, and a high performance DSP core. Our proprietary memory system architecture enables up to 33.2 gigabits per second of bandwidth, and our DSP enables processing of image resolutions as high as QXGA, which requires more than 5 gigabits of bandwidth per second. By integrating the microprocessor and peripherals, memory, and DSP our products provide a complete solution to the core electronics of a display device.

BROAD INTERFACE FLEXIBILITY. Our ImageProcessor ICs work with analog or digital input sources, ranging from VGA to QXGA computer graphics resolutions, and the latest HDTV video.

Pixelworks Integrates Up To 10 Chips Onto A Single Chip



COMPLETE SOFTWARE DEVELOPMENT ENVIRONMENT. We provide an embedded operating system, source code, and software tools necessary to customize display devices. Our software development environment includes a proprietary Windows based user interface creation tool, GUI Builder, that enables customers to create finished products with a distinct "look and feel." The GUI Builder also allows our customers to easily create multiple differentiated products. In addition to controlling the user interface our software forms the heart of the real time system at the core of any modern display product. Our software provides a consistent development platform that is portable across product lines and product categories. For example, a customer that develops a projector product that uses our software can easily port that software to a monitor. This benefits the customer by dramatically reducing time to market and providing a unique "look and feel" that delivers a consistent customer experience across an entire product portfolio.

INTELLIGENT IMAGE PROCESSING TECHNOLOGY

Our technology supports multi-standard analog and digital video, including digital television or DTV, HDTV, National Television Standards Committee, or NTSC, PAL and SECAM. Our intelligent image processing solution simplifies the use and development of display devices. Features of our technology include the following:

IMAGE SCALING AND SHAPING Our image processing technology incorporates a proprietary programmable two-dimensional image scaler capable of resizing images to fit a wide variety of aspect ratios, the ratio of width to height of display screens, and resolutions. With our scaler, images can be adapted to aspect ratios ranging from traditional 4:3 aspect ratios of conventional computer monitors and televisions to the 16:9 format used in wide screen HDTVs. In addition, content designed for a certain resolution can be intelligently stretched or reduced in real time to fit a new resolution for a specific display without degrading the image. For example low-resolution images are processed by intelligently adding information, so that when the new image is displayed, it looks smooth without any jagged image areas. High-resolution content can be displayed on lower resolution displays by intelligently removing information without degrading image quality.

Our technology allows the shape of an image to be changed in multiple dimensions. This is useful in compensating for optical distortions in products such as front projection systems and rear projection televisions. For example, standard resolution videotapes designed for conventional television display can be resized and formatted for display on a high-resolution wide-screen flat panel television without degrading the image. This capability is increasingly important as HDTV becomes more prevalent. HDTV content can be delivered in as many as 18 different combinations of resolutions and aspect ratios. Our technology is also useful in compensating for optical distortions introduced by the lenses used in products such as front projection systems and rear projection TVs.

ADAPTIVE IMAGE OPTIMIZATION. Our products must interface to a broad array of standard and non-standard protocols. As a result, intelligent methods of acquiring and identifying a signals format must be used. We use a proprietary image processing circuit that can automatically determine the key parameters of an arbitrary input signal and through our software drivers configure the system to produce the best possible image. Our adaptive image optimization technology automatically adjusts incoming signals to achieve the highest possible image quality. The display adjusts itself when it is turned on and continuously adjusts with every change of the incoming signals to display an optimal image.

ADVANCED VIDEO PROCESSING. Flat panel displays are progressive scan devices. Images are built and displayed sequentially one row or line at time. Typically, video signals are interlaced or built using every other row. First the odd rows are displayed and then the image is updated with the even rows. Our image processing technology converts the incoming interlaced video signals for display on flat panels by doubling the incoming signals to match the progressive scan capabilities of flat panel displays. This is an especially difficult challenge. Simply merging the odd and even fields results in very jagged image edges. Our intelligent approach uses a sophisticated video digital signal processing technique to display the best possible image.

COLOR COMPENSATION TECHNOLOGY. Our sophisticated custom color compensation technology makes it possible to display consistent color images from video and computer graphics, which use very different color palettes, on different display devices. Our color processing technology compensates for variations in the color performance of a display. Using our unique approach any color can be addressed independently and adjusted without impacting other colors. Our customers can use our color compensation technology to compensate for non-uniform color in a specific display and to provide consistent color performance across multiple products using different display technologies. It can also be used to compensate for color variations in display components provided by different vendors.

Our non-linear color compensation technology allows precise color matching and may enable products which can precisely represent the color of the original source. The applications of this technology include graphic design where colors on a display using an ImageProcessor IC can be accurately matched to a print output. Another application is for improving end-user satisfaction when using Internet e-commerce shopping sites by enabling exact color representation of products to be shown on a display.

FULLY CUSTOMIZABLE ON-SCREEN DISPLAY

Our technology couples an integrated on-screen display controller with a unique Windows-based application that allows customers who are designing ImageProcessor ICs into their display products to quickly develop and implement their own unique user interfaces that can incorporate graphics and colorful icons to support branding in start-up displays and menus.

CUSTOMIZABLE FEATURE SUPPORT FOR SPECIFIC DEVICE FUNCTIONALITY

This allows developers to add unique features for specific devices. Customizable features currently include:

- Picture-in-picture for products in the consumer multimedia, high-end desktop monitors and business presentation markets

- Image shaping for keystone correction in business presentation products

- Digital zoom to enlarge images electronically

MIXED SIGNAL SUPPORT

Our ImageProcessor ICs can support as many as four different input sources to be displayed on a single device through integrated and add-on analog and digital receivers and connectors. Analog computer graphics, TMDS digital graphics supporting the DVI standard and video through composite and S-Video sources can be captured, decoded and optimized.

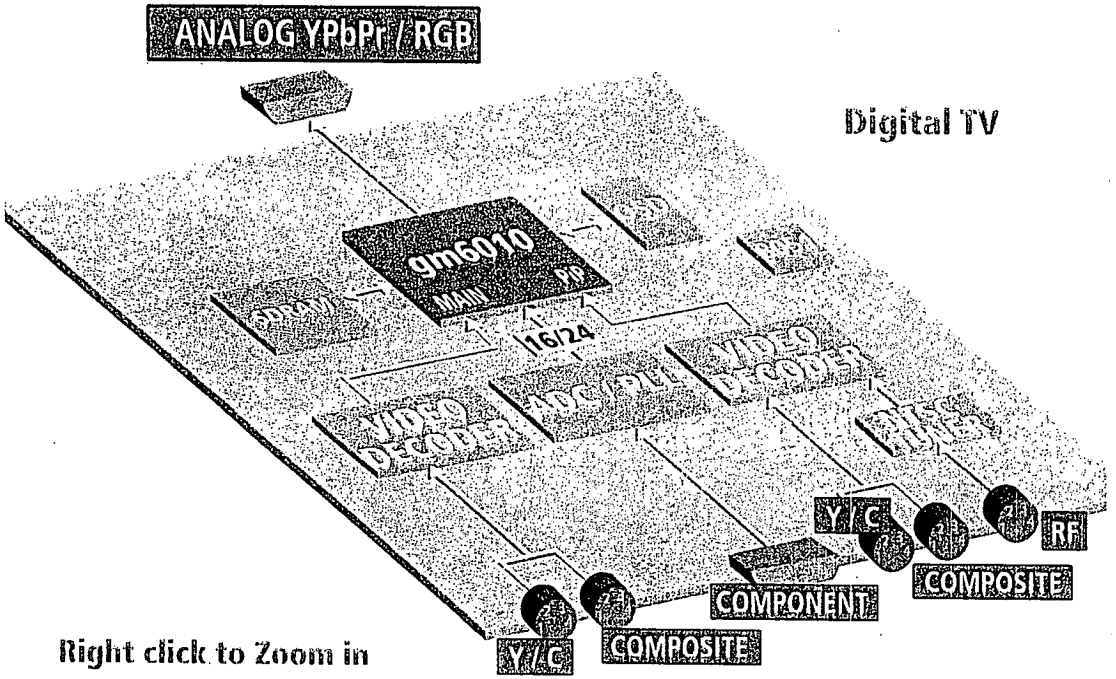
GENESIS Any Source Any Display
DISPLAY PERFECTION

gm6010 Digital TV Controller

The gm6010 digital TV controller is the industry's most highly integrated video-processing IC for DTV, HDTV and HDTV-ready consumer televisions. Featuring Genesis's Crystal CinemaTM video scan conversion, the gm6010 excels at up-converting standard definition video to higher-resolution, enhanced display formats. The gm6010 integrates dual-channel video processing (MAIN and PIP), SDRAM controller, color controls, look-up table, mixer, PiP/PoP/multi-PiP and triple 10-bit DACs. The rich feature set of the gm6010 is controlled via a powerful register-based programming model that combines flexibility with ease of use. Ideally suited for progressive and HD direct-view CRT televisions, the gm6010 enables consumer television manufacturers to offer a cinema-like TV viewing experience from standard-definition interlaced video inputs.

Features

- Crystal Cinema^{TM} Video scan conversion
- High-quality de-interlacing, interlacing
- Programmable arbitrary scaling (shrink/zoom)
- Film detection and 2:2/3:2 inverse pull-down optimized for TV
- Format conversion (anamorphic, letterbox, panoramic)
- Dual-channel digital YCbCr/GBR inputs up to HD 1080i
- Analog YpbPr/GBR outputs up to HD 1080i with bi/tri level or TTL sync
- PiP/PoP, twin picture, multi-PiP



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Title	Filename	Size	Date
gm6010/15/20 Digital TV Controller Product Brief	C6010-PBR-01H.PDF	746kb	Feb 2002

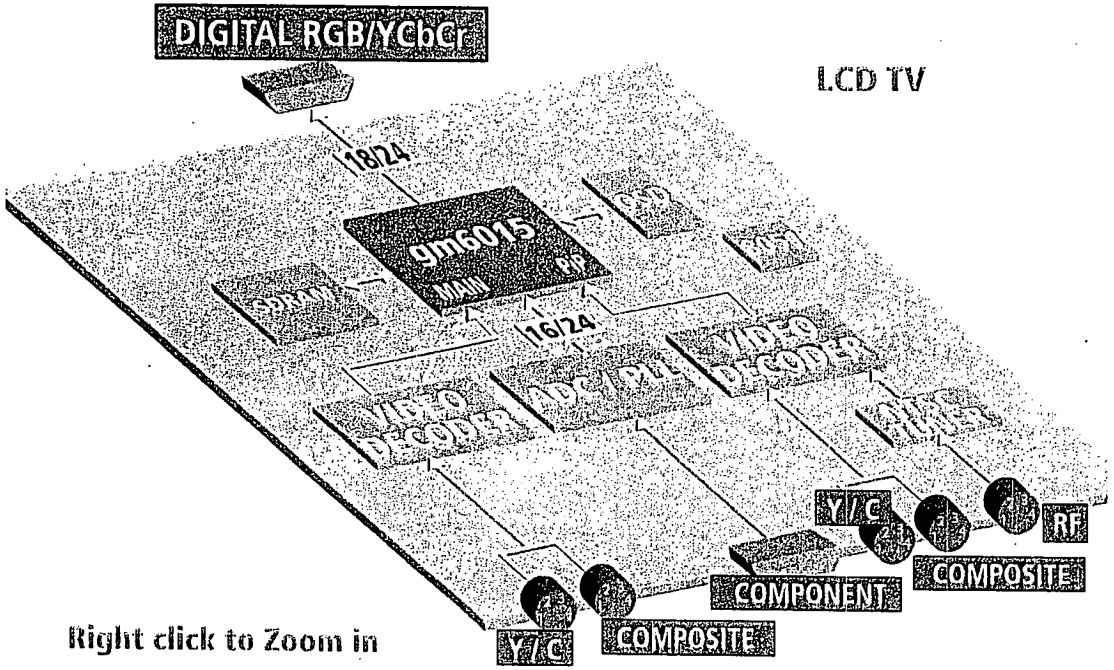
Any Source Any Display
DISPLAY PERFECTION

gm6015 LCD-TV Controller

Designed for consumer televisions requiring a digital interface to the display subsystem, the gm6015 LCD TV controller is ideally suited for televisions employing LCD, LCOS and PDP display technologies. Featuring Genesis's Crystal CinemaTM video scan conversion, the gm6015 integrates dual-channel processing (MAIN and PIP), SDRAM controller, color controls, look-up table, mixer, PiP/PoP/multi-PIP and digital video outputs. The gm6015 excels at up-converting standard-definition interlaced video to XGA and HD 720p display formats. The rich feature set of the gm6015 is controlled via an advanced register-based programming model.

Features

- Crystal Cinema^{TM} video scan conversion
- High quality de-interlacing, interlacing
- Programmable arbitrary scaling (shrink/zoom)
- Film detection and 2:2/3:2 inverse pull-down optimized for TV
- Format conversion (anamorphic, letterbox, panoramic)
- Dual channel digital YCbCr/GBR inputs up to HD 1080i
- 8/16/18/24/30-bit YCbCr/GBR digital video outputs up to HD 720p
- PiP/PoP, twin picture, multi-PiP



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Title	Filename	Size	Date
gm6010/15/20 Digital TV Controller Product Brief	C6010-PBR-01H.PDF	746kb	Feb 2002

Reference AI

DPTV™-iX

Preliminary
Product Brief

OVERVIEW

The DPTV-iX is the main component in the premier TV chipset solution on the market. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV-iX can accept HDTV broadcast through a direct MPEG2 interface. Trident's DPTV™ product family propels the corporate mission of *Digital Media For The Masses* by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Interlaced and Progressive Scan refresh
- ✧ 13 Dynamic picture quality enhancements (13D)
- ✧ PAL/NTSC/SECAM TV decoder with programmable 5 Tap adaptive comb filter
- ✧ VBI/Closed Caption
- ✧ Optional Text/Graphical OSD capability
- ✧ MPEG2 Digital Video Interface
- ✧ SVGA digital/analog overlay with OSD and PIP
- ✧ PIP, POP, multi-picture , and panorama display modes
- ✧ Programmable Zoom Viewer
- ✧ Linear and non-Linear scaling
- ✧ Gamma Correction and Alpha Blending
- ✧ Supports high speed, low cost Frame Buffer
- ✧ Advanced Mixed-Signal Processing with 0.35µm process
- ✧ Single chip: 208 PQFP

Interlaced and Progressive Scan Refresh

- Interlaced @ 60Hz to 100 Hz

TV Decoder With Programmable 5 Tap Adaptive Comb Filter

- Supports NTSC, PAL and SECAM formats.
- Analog Front-end with dual 10-bit ADC
- Comb filter is programmable to 0, 3 & 5 taps to adapt to all possible environments.

13D: Dynamic Picture Enhancements

- Dynamic Lumiance Transience Index
- Dynamic Chromance Transience Index
- Dynamic Scan Velocity Modulation
- Dynamic Digital Comb Filter
- Dynamic Temporal frame-Filtering Noise Reduction
- Dynamic Gamma Control
- Dynamic Black Level eXtender
- Dynamic Brightness/Contrast Adjustment
- Dynamic Adaptive Smoothing Filter
- Dynamic Frame/Scan Rate Converter
- Dynamic White Peak Level Restriction
- Dynamic Room Temperature Color Correction
- Dynamic Digital SVGA Overlay

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Picture-in-Picture (PIP). Available with 16 different color framing for maximizing viewing experience. PIP window is reposition-able to suit viewers personal preference/habits.
- Picture-Out-Picture (POP), multi-picture, Cinema 1 and Cinema 2 are some forms of dual program screening supported by the advanced architecture of the DPTV. For multi-picture viewing, the screen is divided evenly as 4 or 9 smaller screens.
- Panorama viewing is best supported on a 16:9 aspect ratio screen, and is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing may be available.

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling algorithms are applied to maximize the viewing experience in the various display modes.
- Programmable Zoom Viewer. Allows partial still pictures and live broadcast to be viewed in greater detail. This feature uses technology available in the PIP and OSD features of the DPTV-iX.
- Alpha blending and overlay. The real world is composed of transparent, translucent, and opaque objects. Resulting objects of a picture that is alpha blend processed will have higher clarity and definition, while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.

- Picture controls-hue, saturation, brightness, contrast. Using dynamic picture enhancement techniques, the DPTV-iX could automatically adjusts these parameters to its optimal balance.

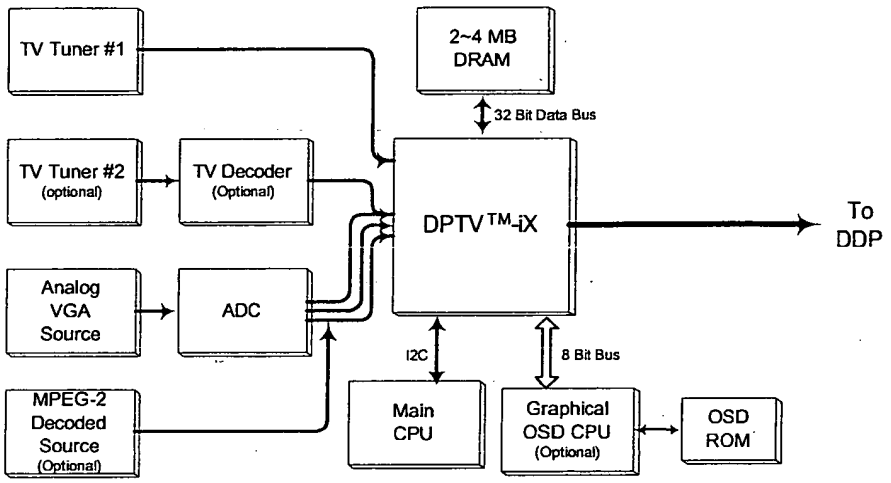
Inputs / Outputs

- One direct TV tuner video signal input
- One secondary TV tuner video signal input, through external TV decoder.
- Alternative (shared input) SVGA/MPEG-2 digital video input
- Component Input
- Composite Video
- S-Video

Packaging

- 208 PQFP
- Ordering part number is 6610

Trident DPTV™-iX Solution



- Trident's DPTV™ solution supports two TV sources. An NTSC/PAL TV decoder with 5 tap adaptive comb filter is integrated to enhance the quality of the display picture.
- Enhanced Video features such as POP, Cinema 1, Cinema 2, OSD , etc., is controlled through the Micro-Controller.
- Minimum Frame Buffer RAM is 2MB for normal operations, and 4MB if Panorama, De-interlacing or other advanced features are used.

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Trident Microsystems, Inc. 2450 Walsh Avenue Santa Clara, CA 95051-1303 USA Phone: (408)-496-1085 Fax: (408) 496-6473 Web site: http://www.tridentmicro.com	Trident Microsystems (Far East), LTD. Taiwan Branch 18F, No. 202, Sec 2 Yen Ping North Road Taipei, Taiwan, ROC Phone: 886-2-2550-6616 Fax: 886-2-2550-3901	Trident Microsystems (Far East), LTD. Unit , 18F Tower 2 Enterprise Square 9 Sheung Yuet Road, Kowloon Bay Kowloon, Hong Kong Phone: 856-2756-9666 Fax: 856-2796-9849

DPTV™-HX

Preliminary
Product Brief

OVERVIEW

The DPTV-HX is the main component in the premier TV chipset solution on the market. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV-HX converts today's analog TV into an advanced progressive TV quality. It also accepts HDTV broadcast through a direct MPEG2 interface. Trident's DPTV™ product family propels the corporate mission of *Digital Media For The Masses* by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Interlaced and Progressive Scan refresh
- ✧ 13 Dynamic picture quality enhancements (13D)
- ✧ PAL/NTSC/SECAM TV decoder with programmable 5 Tap adaptive comb filter
- ✧ VBI/Closed Caption (Optional)
- ✧ Text/Graphical OSD capability (Optional)
- ✧ Motion & Edge Adaptive De-interlacing
- ✧ MPEG2 Digital Video Interface
- ✧ Multi-picture and panorama display modes
- ✧ Linear and non-Linear scaling
- ✧ Gamma Correction and Alpha Blending
- ✧ Supports high speed, low cost Frame Buffer
- ✧ Advanced Mixed-Signal Processing with 0.35µm process
- ✧ Single chip: 208 PQFP

Interlaced and Progressive Scan Refresh

- Interlaced @ 60Hz to 100 Hz
- Progressive Scan @ 60 Hz

Motion & Edge Adaptive De-interlacing

- Improves the clarity and sharpness of the overall picture.
- This feature enhances the "slow-moving" portions of the picture by doubling the resolution of those areas. This unique feature is enabled by utilizing Trident's proprietary de-interlacing technology.

TV Decoder With Programmable 5 Tap Adaptive Comb Filter

- Supports NTSC, PAL and SECAM formats.
- Analog Front-end with dual 10-bit ADC
- Comb filter is programmable to 0, 3 & 5 taps to adapt to all possible environments.

13D: Dynamic Picture Enhancements

- Dynamic Lumiance Transience Index
- Dynamic Chromance Transience Index
- Dynamic Scan Velocity Modulation
- Dynamic Digital Comb Filter
- Dynamic Motion & Edge Adaptive De-interlacing
- Dynamic Temporal frame-Filtering Noise Reduction
- Dynamic Gamma Control
- Dynamic Black Level eXtender
- Dynamic Brightness/Contrast Adjustment
- Dynamic Adaptive Smoothing Filter
- Dynamic Frame/Scan Rate Converter
- Dynamic White Peak Level Restriction
- Dynamic Room Temperature Color Correction

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Panorama viewing is best supported on a 16:9 aspect ratio screen, and is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing may be available.

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling algorithms are applied to maximize the viewing experience in the various display modes.
- Alpha blending and overlay. The real world is composed of transparent, translucent, and opaque objects. Resulting objects of a picture that is alpha blend processed will have higher clarity and definition, while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.
- Picture controls-hue, saturation, brightness, contrast. Using dynamic picture enhancement techniques, the DPTV-HX could automatically adjusts these parameters to its optimal balance.

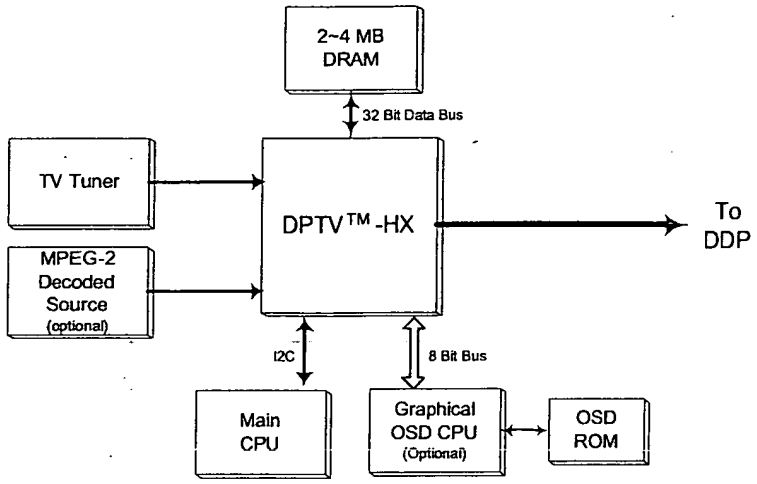
Inputs / Outputs

- One direct TV tuner video signal input
- MPEG-2 digital video input
- Component Input
- Composite Video
- S-Video

Packaging

- 208 PQFP
- Ordering part number is 6620

Trident DPTV™-HX Solution



- Trident's DPTV™ solution supports one TV sources. An NTSC/PAL TV decoder with 5 tap adaptive comb filter is integrated to enhance the quality of the display picture.
- Enhanced Video features such as Cinema 1, Cinema 2, OSD , etc., is controlled through the Micro-Controller.
- Minimum Frame Buffer RAM is 2MB for normal operations, and 4MB if Panorama, De-interlacing or other advanced features are used.

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Trident

DPTV™-DX

Preliminary
Product Brief

OVERVIEW

The DPTV™-DX is the main component in premier TV chipset solutions in the market. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV™-DX converts today's analog TV into an advanced progressive TV quality. It also accepts HDTV broadcast through a direct MPEG2 interface. Trident's DPTV™ product family propels our corporate mission by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Interlaced and progressive scan refresh
- ✧ 14 Dynamic picture quality enhancements (14D)
- ✧ PAL/NTSC/SECAM TV decoder with programmable 5-Tap adaptive comb filter
- ✧ VBI/Closed Caption
- ✧ Optional text/graphical OSD capability
- ✧ Motion & edge adaptive de-interlacing
- ✧ MPEG2 digital video interface
- ✧ SVGA digital/analog overlay with OSD and PIP
- ✧ PIP, POP, multi-picture, and panorama display modes
- ✧ Programmable zoom viewer
- ✧ Linear and non-linear scaling
- ✧ Gamma correction and alpha blending
- ✧ High-speed support and low-cost frame buffer
- ✧ Advanced mixed-signal processing with 0.35µm process
- ✧ Single chip: 208 PQFP

Interlaced and Progressive Scan Refresh

- Interlaced @ 60Hz to 100 Hz
- Progressive scan @ 50 Hz to 75 Hz

Motion & Edge Adaptive De-interlacing

- Improves the clarity and sharpness of the overall picture.
- Enhances the "slow-moving" portions of the picture by doubling the resolution of those areas by utilizing Trident's proprietary de-interlacing technology.

TV Decoder With Programmable 5-Tap Adaptive Comb Filter

- Supports NTSC, PAL and SECAM formats.
- Supports analog front-end with dual 10-bit ADC
- Programs comb filter to 0, 3, & 5 taps to adapt to all possible environments.

14D: Dynamic Picture Enhancements

- Dynamic luminance transience index
- Dynamic chrominance transience index
- Dynamic scan velocity modulation
- Dynamic digital comb filter
- Dynamic motion & edge adaptive de-interlacing
- Dynamic temporal frame-filtering noise reduction
- Dynamic gamma control
- Dynamic black level extender
- Dynamic brightness/contrast adjustment
- Dynamic adaptive smoothing filter
- Dynamic frame/scan rate converter
- Dynamic white peak level restriction
- Dynamic room temperature color correction
- Dynamic digital SVGA overlay

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Picture-in-Picture (PIP). The PIP display mode is available with 16 different color frames for maximizing viewing experience. It can be repositioned to suit personal preferences and habits.
- Picture-Out-Picture (POP), multi-picture, cinema 1, and cinema 2 are some forms of dual program screening supported by the advanced architecture of the DPTV. For multi-picture viewing, the screen is divided evenly into 4 or 9 smaller screens.
- Panorama viewing is best supported on a 16:9 aspect ratio screen. It is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing are also available.

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling algorithms are applied to maximize the viewing experience in the various display modes.
- The programmable zoom viewer allows partial still pictures and live broadcast to be viewed in greater detail. This feature uses technology available in the PIP and OSD features of the DPTV™-DX.
- Alpha blending and overlay results in higher clarity

and definition of objects of a picture while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.
- Picture controls such as hue, saturation, brightness, and contrast can be automatically adjusted to their optimal balance using dynamic picture enhancement techniques.

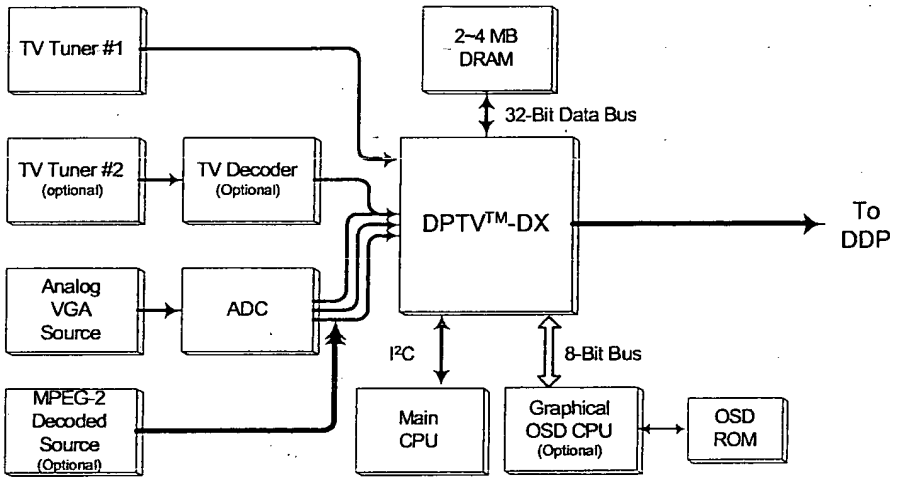
Inputs / Outputs

- One direct TV tuner video signal input
- One secondary TV tuner video signal input, through external TV decoder.
- Alternative (shared input) SVGA/MPEG-2 digital video input
- Component input
- Composite video input
- S-Video input

Packaging

- 208-Pin PQFP
- Ordering part number is 6630

Trident DPTV™-DX Solution



- Trident's DPTV™ solution supports two TV sources. An NTSC/PAL TV decoder with 5-tap adaptive comb filter is integrated to enhance the quality of the display picture.
- Enhanced video features such as POP, Cinema 1, Cinema 2, OSD, etc., are controlled through the micro-controller.
- Minimum frame buffer RAM is 2MB for normal operations, and 4MB if panorama, de-interlacing or other advanced features are used.

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Trident

DPTV™-MVS

Preliminary
Product Brief

OVERVIEW

The DPTV™-MVS is a high performance digital video-processing chip for progressive DVD player and TV applications. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Progressive Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV™-MVS supports CCIR-656, CCIR-606 digital input signals and directly interfaces with most common video decoders seamlessly. It is the ideal de-interlacing chip for a progressive DVD Player or as the format converter in a HDTV set top box design. Trident's DPTV™ product family propels our corporate mission by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Film mode recovery for movie titles
- ✧ Frequency rate conversion for different output display devices
- ✧ 14 Dynamic picture quality enhancements (14D)
- ✧ VBI/Closed Caption
- ✧ Optional text/graphical OSD capability
- ✧ Motion & edge adaptive de-interlacing
- ✧ MPEG2 digital video interface
- ✧ SVGA digital/analog overlay with OSD and PIP
- ✧ PIP, POP, multi-picture, and panorama display modes
- ✧ Programmable zoom viewer
- ✧ Linear and non-linear scaling
- ✧ Gamma correction and alpha blending
- ✧ High-speed support and low-cost frame buffer
- ✧ Integrated DAC for direct analog RGB or YPbPr output
- ✧ Multiple output formats for 480P, 720P, or 1080I
- ✧ Built-in 10-bit DAC
- ✧ Optional 20-bit Y/C interface for external DAC
- ✧ Audio/Video lip synchronization
- ✧ Advanced mixed-signal processing with 0.25 µm process
- ✧ Easy upgrade to DPTV™-DX design with an internal color decoder
- ✧ Single chip: 208 PQFP

Progressive Scan Refresh

- Progressive scan @ 50 Hz to 75 Hz

Motion & Edge Adaptive De-interlacing

- Improves the clarity and sharpness of the overall picture.
- Enhances feature enhances the "slow-moving" portions of the picture by doubling the resolution of those areas by utilizing Trident's proprietary de-interlacing technology.

14D: Dynamic Picture Enhancements

- Dynamic luminance transience index
- Dynamic chrominance transience index
- Dynamic scan velocity modulation
- Dynamic digital comb filter
- Dynamic motion & edge adaptive de-interlacing
- Dynamic temporal frame-filtering noise reduction
- Dynamic gamma control
- Dynamic black level extender
- Dynamic brightness/contrast adjustment
- Dynamic adaptive smoothing filter
- Dynamic frame/scan rate converter
- Dynamic white peak level restriction
- Dynamic room temperature color correction
- Dynamic digital SVGA overlay

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Picture-in-Picture (PIP). The PIP display mode is available with 16 different color frames for maximizing viewing experience. It can be repositioned to suit personal preferences and habits.
- Picture-Out-Picture (POP), multi-picture, cinema 1, and cinema 2 are some forms of dual program screening supported by the advanced architecture of the DPTV™. For multi-picture viewing, the screen is divided evenly into 4 or 9 smaller screens.
- Panorama viewing is best supported on a 16:9 aspect ratio screen. It is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing are also available.

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling

algorithms are applied to maximize the viewing experience in the various display modes.
- The programmable zoom viewer allows partial still pictures and live broadcast to be viewed in greater detail. This feature uses technology available in the PIP and OSD features of the DPTV™-MVS.
- Alpha blending and overlay results in higher clarity and definition of objects of a picture while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.
- Picture controls such as hue, saturation, brightness, and contrast can be automatically adjusted to their optimal balance using dynamic picture enhancement techniques.

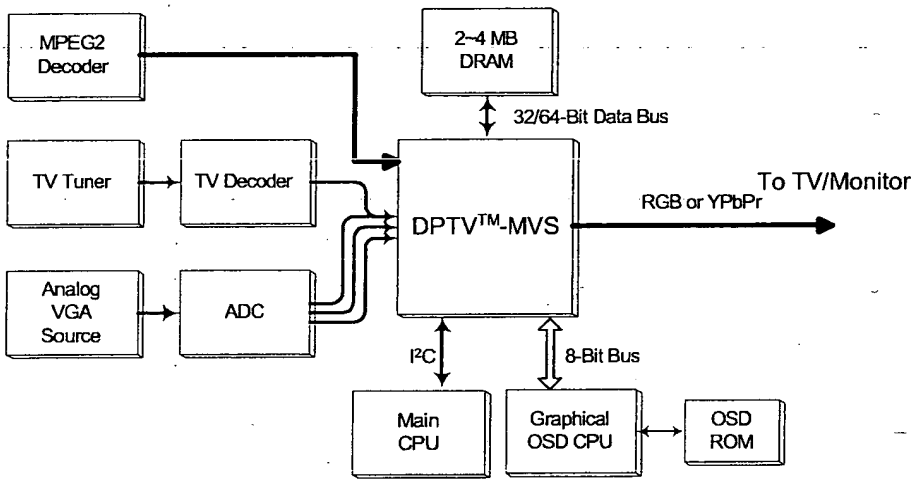
Inputs / Outputs

- MPEG-2 digital video input
- Composite, component or S-Video Input through an external TV decoder.
- Analog SVGA input though an external ADC.
- Supports YPbPr output with 525P copy protection
- Analog RGB or YPbPr for 480P/720P/1080i progressive output

Packaging

- 208-Pin PQFP.
- Ordering part number is 6740

Trident DPTV™-MVS Solution



- Trident's DPTV™ solution supports two input sources. A direct MPEG2 digital video input and a TV input through an external decoder. The second input source can be from analog SVGA through an external DAC.
- Enhanced video features such as POP, Cinema 1, Cinema 2, OSD, etc., are controlled through the micro-controller.
- Minimum frame buffer RAM is 2MB for normal operations, and 4MB if panorama, de-interlacing, or other advanced features are used.

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Phone: (408) 991-8800 Fax (408) 733-1438 Web site: http://www.tridentmicro.com	Phone: 886-2-2657-7686 Fax 886-2-2627-8727 Web site: http://www.trident.com.tw	Phone: 856-2756-9666 Fax 856-2796-9849

Trident

DPTV™-MV

Preliminary
Product Brief

OVERVIEW

The DPTV™-MV is the main component in the premier TV chipset solution on the market. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV™-MV converts today's analog TV into an advanced progressive TV quality. Decoded HDTV digital video streams can be formatted to different output display modes by DPTV™. Trident's DPTV™ product family propels our corporate mission by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Film mode recovery for movie titles
- ✧ Interlaced and progressive scan refresh
- ✧ 14 Dynamic picture quality enhancements (14D)
- ✧ Advanced PAL/NTSC/SECAM TV decoder with programmable 5-Tap adaptive comb filter
- ✧ VBI/Closed Caption
- ✧ Optional text/graphical OSD capability
- ✧ Motion & edge adaptive de-interlacing
- ✧ MPEG2 digital video interface
- ✧ SVGA digital/analog overlay with OSD and PIP
- ✧ PIP, POP, multi-picture, and panorama display modes
- ✧ Programmable zoom viewer
- ✧ Linear and non-linear scaling
- ✧ Gamma correction and alpha blending
- ✧ High-speed support and low-cost frame buffer
- ✧ 10-bit ADC front end and 10-bit DAC
- ✧ Advanced digital noise reduction for chroma and luma
- ✧ Audio/Video lip synchronization
- ✧ Advanced mixed-signal processing with 0.25µm process
- ✧ Single chip: 208 PQFP

Interlaced and Progressive Scan Refresh

- Interlaced @ 60Hz to 100 Hz
- Progressive Scan @ 50 Hz to 75 Hz

Motion & Edge Adaptive De-interlacing

- Improves the clarity and sharpness of the overall picture.
- Enhances the "slow-moving" portions of the picture by doubling the resolution of those areas by utilizing Trident's proprietary de-interlacing technology.
- Enables film mode recovery for movie titles

Advanced digital TV Decoder With Programmable 5-Tap filter

- Supports NTSC, PAL and SECAM formats.
- Supports analog front-end with dual 10-bit ADC
- Programs comb filter to 0, 3, & 5 taps to adapt to all possible environments.

14D: Dynamic Picture Enhancements

- Dynamic luminance transience index
- Dynamic chrominance transience index
- Dynamic scan velocity modulation
- Dynamic digital comb filter
- Dynamic motion & edge adaptive de-interlacing
- Dynamic temporal frame-filtering noise reduction
- Dynamic gamma control
- Dynamic black level extender
- Dynamic brightness/contrast adjustment
- Dynamic adaptive smoothing filter
- Dynamic frame/scan rate converter
- Dynamic white peak level restriction
- Dynamic room temperature color correction
- Dynamic digital SVGA overlay

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Picture-in-Picture (PIP). The PIP display mode is available with 16 different color frames for maximizing viewing experience. It can be repositioned to suit personal preferences and habits.
- Picture-Out-Picture (POP), multi-picture, cinema 1, and cinema 2 are some forms of dual program screening supported by the advanced architecture of the DPTV. For multi-picture viewing, the screen is divided evenly into 4 or 9 smaller screens.
- Panorama viewing is best supported on a 16:9 aspect ratio screen. It is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing are also available.

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling

algorithms are applied to maximize the viewing experience in the various display modes.
- The programmable zoom viewer allows partial still pictures and live broadcast to be viewed in greater detail. This feature uses technology available in the PIP and OSD features of the DPTV™-MV
- Alpha blending and overlay results in higher clarity and definition of objects of a picture while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.
- Picture controls such as hue, saturation, brightness, and contrast can be automatically adjusted to their optimal balance using dynamic picture enhancement techniques.

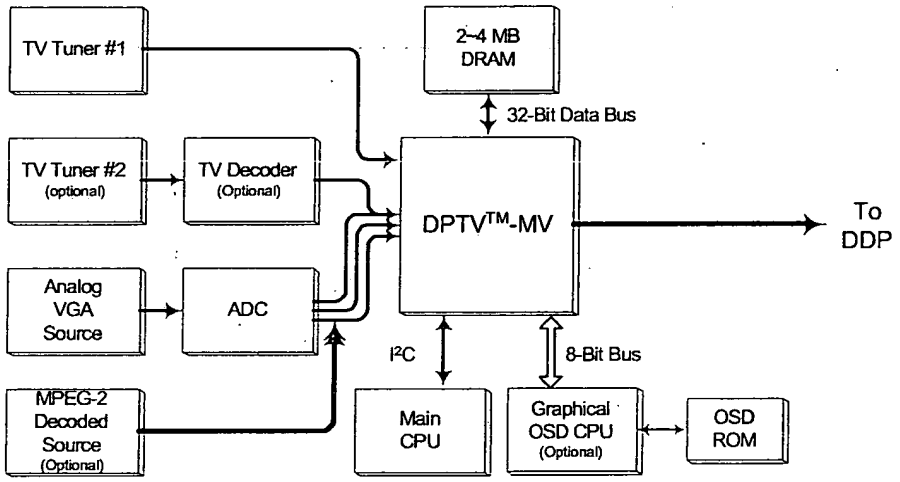
Inputs / Outputs

- One direct TV tuner video signal input
- One secondary TV tuner video signal input, through external TV decoder.
- Alternative (shared input) SVGA/MPEG-2 digital video input
- Component input
- Composite video input
- S-Video input
- Direct YPbPr output with 525P copy protection

Packaging

- 208-Pin PQFP
- Ordering part number is 6720

Trident DPTV™-MV Solution



- Enhanced video features such as POP, Cinema 1, Cinema 2, OSD, etc., are controlled through the Micro-Controller.
- Minimum frame buffer RAM is 2MB for normal operations, and 4MB if panorama, de-interlacing or other advanced features are used.

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Trident

DPTV™-3D

Preliminary
Product Brief

OVERVIEW

The DPTV™-3D is the main component in premier TV chipset solutions in the market. Designed for maximum system design flexibility, users of Trident's single chip DPTV™ Video Processor(s) will benefit from one of the most feature rich devices available while maintaining a price competitive advantage over the existing solution(s). The DPTV™-3D converts today's analog TV into an advanced progressive TV quality. Decoded HDTV digital video streams can be formatted into different output display modes by DPTV™. Trident's DPTV™ product family propels our corporate mission by delivering tomorrow's digital media technology to today's consumer.

FEATURES

- ✧ Adaptive 3D digital comb filter
- ✧ Film mode recovery for movie titles
- ✧ Interlaced and progressive scan refresh
- ✧ 14 Dynamic picture quality enhancements (14D)
- ✧ PAL/NTSC/SECAM TV decoder with programmable 5-Tap adaptive comb filter
- ✧ VBI/Closed Caption
- ✧ Optional text/graphical OSD capability
- ✧ Motion & edge adaptive de-interlacing
- ✧ MPEG2 digital video interface
- ✧ SVGA digital/analog overlay with OSD and PIP
- ✧ PIP, POP, multi-picture, and panorama display modes
- ✧ Programmable zoom viewer
- ✧ Linear and non-linear scaling
- ✧ Gamma correction and alpha blending
- ✧ High-speed support and low-cost frame buffer
- ✧ 10-bit ADC front end and 10-bit DAC
- ✧ Advanced digital noise reduction for chroma and luma
- ✧ Audio/video lip synchronization
- ✧ Advanced mixed-signal processing with 0.25µm process
- ✧ Single chip: 208 PQFP

Interlaced and Progressive Scan Refresh

- Interlaced @ 60Hz to 100 Hz
- Progressive scan @ 50 Hz to 75 Hz

Motion & Edge Adaptive De-interlacing

- Improves the clarity and sharpness of the overall picture.
- Enhances the "slow-moving" portions of the picture by doubling the resolution of those areas by utilizing Trident's proprietary de-interlacing technology.
- Enables film mode recovery for movie titles

Adaptive 3D digital TV Decoder With Programmable 5-Tap filter

- Supports NTSC, PAL and SECAM formats.
- Supports analog front-end with dual 10-bit ADC
- Includes adaptive 3D digital comb filter
- Programs comb filter to 0, 3, & 5 taps to adapt to all possible environments.

14D: Dynamic Picture Enhancements

- Dynamic luminance transience index
- Dynamic chrominance transience index
- Dynamic scan velocity modulation
- Dynamic digital comb filter
- Dynamic motion & edge adaptive de-interlacing
- Dynamic temporal frame-filtering noise reduction
- Dynamic gamma control
- Dynamic black level extender
- Dynamic brightness/contrast adjustment
- Dynamic adaptive smoothing filter
- Dynamic frame/scan rate converter
- Dynamic white peak level restriction
- Dynamic room temperature color correction
- Dynamic digital SVGA overlay

OSD and (optional) VBI / Closed Caption

- Vertical Blank Interval (VBI) is a new industry standard for transmitting non-video data over the TV broadcast signal during the dead time (Vertical Blanking). Close-captioned information is one of the non-video data that uses this portion of the transmission time.
- On-Screen Display (OSD). Users can choose to implement text-based OSD through the main CPU, or graphical-based OSD through an optional OSD CPU.

Screen Display Modes

- Picture-in-Picture (PIP). The PIP display mode is available with 16 different color frames for maximizing viewing experience. It can be repositioned to suit personal preferences and habits.
- Picture-Out-Picture (POP), multi-picture, cinema 1, and cinema 2 are some forms of dual program screening supported by the advanced architecture of the DPTV. For multi-picture viewing, the screen is divided evenly into 4 or 9 smaller screens.
- Panorama viewing is best supported on a 16:9 aspect ratio screen. It is also supported on a 4:3 aspect ratio screen by downsizing the picture to fit the screen width. Other forms of downsizing are also available.

Trident

DPTV™-3D

Preliminary
Product Brief

Advanced Picture Processing

- Advanced linear and non-linear panorama scaling algorithms are applied to maximize the viewing experience in the various display modes.
- The programmable zoom viewer allows partial still pictures and live broadcast to be viewed in greater detail. This feature uses the technology available in the PIP and OSD features of the DPTV™-3D.
- Alpha blending and overlay results in higher clarity and definition of objects of a picture while maintaining a more natural "look and feel" as it accounts for foreground and background colors.
- Gamma correction.
- Picture controls such as hue, saturation, brightness, and contrast can be automatically adjusted to their optimal balance.

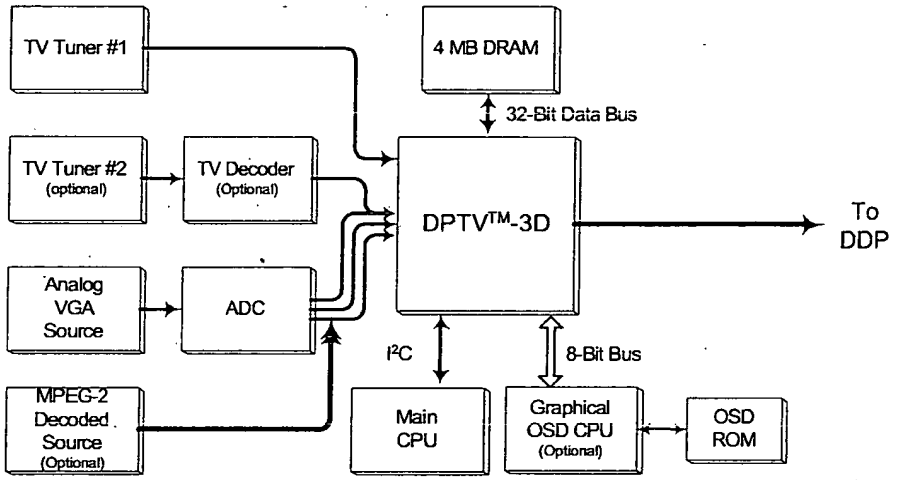
Inputs / Outputs

- One direct TV tuner video signal input
- One secondary TV tuner video signal input, through external TV decoder.
- Alternative (shared input) SVGA/MPEG-2 digital video input
- Component Input
- Composite Video Input
- S-Video Input
- Direct YPbPr output with 525P copy protection

Packaging

- 208-Pin PQFP
- Ordering part number is 6730

Trident DPTV™-3D Solution



- Enhanced video features such as POP, Cinema 1, Cinema 2, OSD, etc., are controlled through the Micro-Controller.
- Minimum frame buffer RAM is 4MB for normal 3D operations, panorama, de-interlacing or other advanced features.

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Reference AT

FLI2300

Digital Video Format Converter

Product Brief

May 2002, doc C0702-PBR-01A

The FLI2300 is a highly integrated digital video format converter for DTV and DVD applications using patented deinterlacing and post processing algorithms from Faroudja Laboratories, coupled with highly flexible scaling, a wide variety of aspect ratio conversions, and other special video enhancing features to produce the highest quality image.

INPUTS –

- Input all industry standard and non-standard video resolutions, including 480i (NTSC), 576i (PAL/SECAM), 480p, 720p, 1080i, and VGA to SXGA
- Digital input, 8-bit Y/Cr/Cb (ITU-R BT656), 8-bit Y/Pr/Pb, 16-bit Y Cr/Cb (ITU-R BT601), 24-bit RGB, YCrCb, YPrPb
- Input pixel rate up to 75 MHz maximum

OUTPUTS –

- Output resolutions include 480p, 576i, 576p, 720p, 1080i, 1080p, and VGA to SXGA
- Interlaced or Progressive output
- Output can be either analog YUV/RGB (through the integrated 10-bit DAC), or digital 24-bit RGB, YCrCb, YPrPb (4:4:4), or digital 16/20-bit Y Cr/Cb (4:2:2)
- Output pixel rate up to 150 MHz maximum

FRONT END PROCESSING –

- Motion Adaptive Noise Reduction - Improves picture quality for off-air material.
- Cross Color Suppressor (CCS) - Removes cross color artifacts in composite video signals due to poor Y/C separation in standard 2D video decoders, eliminating the need for expensive 3D video decoders.

FORMATS –

- Input color manipulation matrix supports all color spaces: RGB, YPrPb, 4:4:4 YCrCb, 4:2:2 YCr/Cb, ITU-R BT656, ITU-R BT601
- Output supports analog RGB, YPrPb, YCrCb, and digital RGB, YPrPb, 4:4:4 YCrCb, 4:2:2 YCr/Cb

DEINTERLACING –

- Per-pixel Motion Adaptive Deinterlacing
- Patented FilmMode Processing - Used for proper de-interlacing of 3:2 and 2:2 pulldown material.
- Edit Correction - Film content is continuously monitored for any break in sequence caused by "bad edits" and quickly compensates for the most effective reduction in artifacts.
- DCDi™ - Video is analyzed on a single pixel granularity to detect presence or absence of angled lines and edges, which are then processed to produce a smooth & natural looking image without visible artifacts or "jaggies".

SCALING –

- High Quality Fully Programmable Two Dimensional Scaler
- Aspect Ratio Conversion for "Anamorphic" or "Panoramic" (non-linear)
- Display 4:3 images on 16:9 displays and vice versa, including Letterbox to Fullscreen, Pillarbox, and Subtitle Display Modes

FRC –

- Tearless Frame Rate Conversion, 50/60/72/75/100/120 Hz.

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1096, 12thA Main, Hal II Stage, Indira Nagar, Bangalore-560 008, India, Tel: (91)-80-526-3878, Fax: (91)-80-529-6245
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143-37 Hyundai Tower, #902, Samsung-dong, Kangnam-gu, Seoul, Korea 135-090 Tel 82-2-553-5693 Fax 82-2-552-4942
Rm2614-2618 Shenzhen Office Tower, 6007 Shennan Blvd, 518040, Shenzhen, Guandong, P.R.C., Tel (0755)386-0101, Fax (0755)386-7874
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www.genesis-microchip.com / info@genesis-microchip.com

MEMORY –

- 32-bit wide SDRAM (i.e. one 2Mx32bit, or two 1Mx16bit), up to 166 MHz operation

SPECIFICATIONS –

- I^2C control interface
- 0.18u technology, 1.8V/3.3V operation
- 208 pin PQFP package
- 525P Macrovision output option (FLI2301 part)

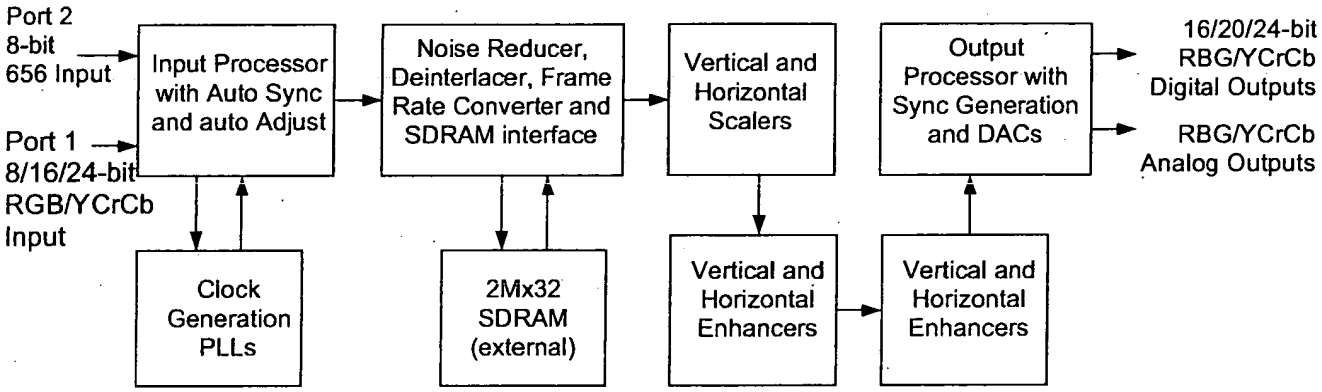
TrueLife™ ENHANCER –

Two dimensional, non-linear, luma & chroma video enhancer brings out details in the picture, producing a more life-like image

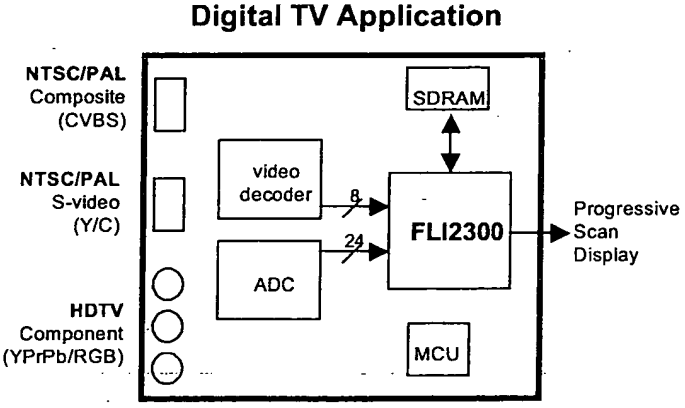
Applications

- Progressive Scan TV
- HD Ready TV / HDTV
- DVD Players
- LCD TV

Chip Block Diagram



System Block Diagram



Reference AK

Product Brief
gm6010 gm6015

C6010-PBR-01H May 2002

Digital TV Controller

DESCRIPTION

The Genesis Microchip gm6010 and gm6015 digital television controller ICs are low-cost, full-featured image processors for progressive TV, digital TV and high-definition TV applications. The gm6010 and gm6015 ICs provide superior image quality by integrating Genesis Crystal Cinema Plus™ video scan conversion with dual digital video inputs (MAIN, PIP), SDRAM controller, color controls, look up table, mixer, multi-image PIP and analog (gm6010) or digital (gm6015) video outputs.

FEATURES

- Genesis industry leading Crystal Cinema Plus™ video scan conversion with:
  - i. Motion adaptive de-interlacing/interlacing
  - ii. 2:2/3:2 film processing
  - iii. Directional Interpolation
  - iv. Arbitrary shrink/zoom scaling
  - v. Aspect ratio conversion
  - vi. Frame rate conversion
  - vii. Spatial, temporal and 3D noise reduction

- Dual-channel MAIN/PIP inputs:
  - i. Up to four 8/16/24-bit 4:2:2/4:4:4 YCbCr/RGB digital video inputs
  - ii. 480/576i, 480/576p, 720p and 1080i
  - iii. VGA, SVGA, XGA, WXGA PC graphics
  - iv. Separate, composite or sync on Y/G

- Display output:
  - i. 8/16/18/20/24/30-bit 4:2:2/4:4:4 YCbCr/RGB digital or analog outputs
  - ii. Triple 256x10 bit output look up table (LUT)
  - iii. Triple 10-bit D/A converters (gm6010)
  - iv. 480/576i, 480/576p, 720p and 1080i HD
  - v. VGA, SVGA, XGA, WXGA PC graphics
  - vi. Separate, composite or sync on Y/G
  - vii. CGMS/A support

FEATURES cont'd

- Frame Rate Conversion:
  - i. Arbitrary frame rate conversion
  - ii. 50/60 Hz → 100/120 Hz field doubling
  - iii. 50 Hz ↔ 60 Hz scan conversion

- Comprehensive PIP Processing:
  - i. PIP/POP with arbitrary size and position
  - ii. Twin Picture/Double Wide support
  - iii. Multi-PIP processing (up to 16 windows)
  - iv. Alpha mixing/overlay between MAIN, PIP and external OSD

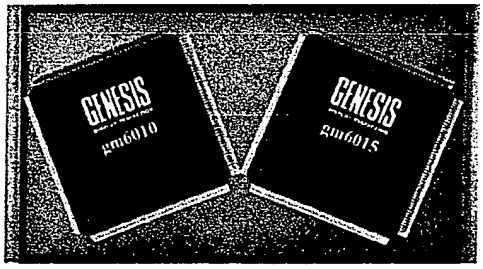
- Other Features:
  - i. Integrated SDRAM controller
  - ii. Single external 2Mx32-bit 100 MHz SDRAM
  - iii. Color controls
  - iv. Serial host interface
  - v. Integrated clock generator and PLLs

PACKAGE

- Low-cost 208-pin PQFP

APPLICATIONS

- CRT, LCD, PDP and LCOS based televisions
- Progressive TV/DTV/HDTV/PTV



NOTES
1. Genesis Display Perfection is a trademark of Genesis Microchip.
2. Crystal Cinema Plus is a trademark of Genesis Microchip.

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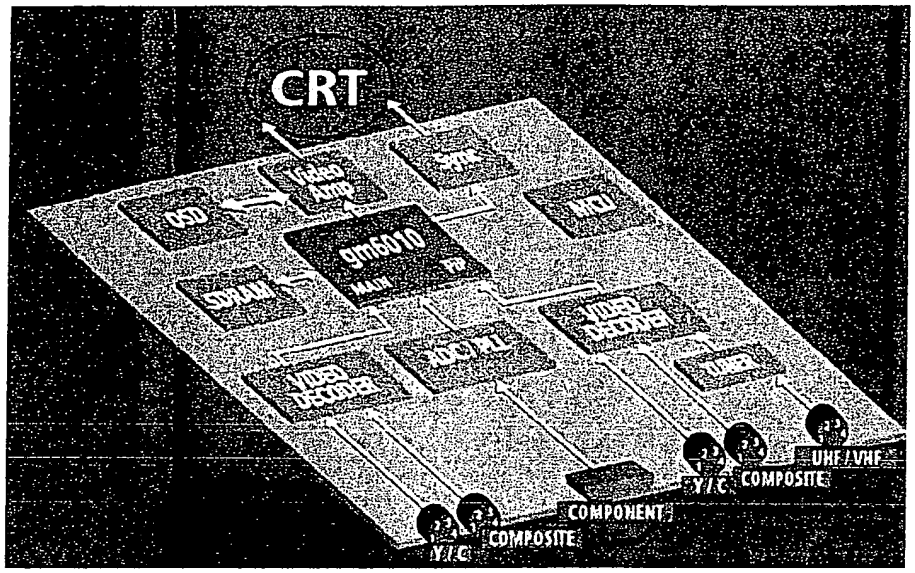
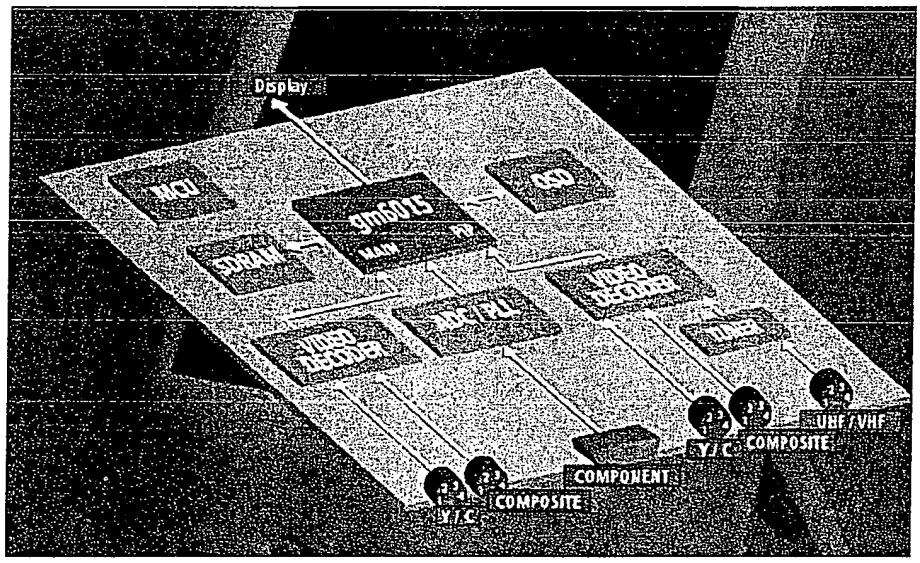
APPLICATION EXAMPLE – HD-READY TV



APPLICATION EXAMPLE – LCD TV



Reference AL

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/150,685	05/17/2002	2811	370	013856-000006	6	11	3

CONFIRMATION NO. 2204

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FILING RECEIPT

OC000000008344740

Date Mailed: 06/25/2002

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

William D. Cox, Chapel Hill, NC;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 06/20/2002

Projected Publication Date: 11/20/2003

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Distributed RAM in a logic array

Preliminary Class

DISTRIBUTED RAM IN A LOGIC ARRAY

BACKGROUND

[0001] For many years, gate arrays have been used to provide quick-turnaround (quick-turn), low non-recurring-expense (NRE) semiconductor devices for a variety of purposes. Traditionally, wafers are processed up to but not including the first (bottom) metal layer, and saved in inventory. When a customer orders a device to be fabricated for a specific application (an application specific integrated circuit or "ASIC"), the customer only pays for the masks to configure the metal layers, and not the transistor layers below. Thus, NRE is reduced. The wafers can be completed quickly, since only the metal layers remain to be fabricated, reducing turn-around time.

[0002] In some of the above-described devices, general purpose, random access memory (RAM) is needed. At one time, to satisfy this need, a separate area of RAM was simply incorporated into the chip. FIG. 1 illustrates such a device. In FIG. 1, blocks of RAM, 100, are incorporated onto chip 102, together with the gate array logic transistors, 104. Metal layers 105 are provided on top of the chip for routing the gate array logic, and the chip is provided with connection pads 106.

[0003] Recently more and more layers of metal have been incorporated into gate array semiconductor devices. Rather than two or three layers of metal, six to eight layers of metal is now common. As a result, gate arrays are no longer very low-NRE, or quick-turn. In order to regain the advantages of earlier gate arrays, several vendors have developed logic arrays, consisting of multiple, substantially identical

logic cells, which can be configured for an application with either fewer or cheaper masks. In the case of fewer masks, the total number of metal layers and hence masks used to create the finished device often does not change. Rather, only a reduced subset of the total number of metal layers in a finished device is used to impart the custom configuration to the device. For example, so-called "one-mask" devices, in which only a single metal layer and hence a single mask imparts customization, can reduce both NRE and turn-time. A side-effect of such techniques is that more area is required in order to complete routing. This naturally leads to a mismatch in the metal area required for routing and the transistor area required to implement logic – extra, unused semiconductor is left in the device. The logic cells in the device are referred to as being "metal-limited."

[0004] FIG. 2 illustrates the semiconductor layer of a metal-limited device 200. The device consists of an array of identical cells, as shown at 202. In each cell only a portion of the semiconductor, for example the portion shown at 204, is used.

[0005] Various ideas have been proposed to make use of the extra silicon in the cells of these metal-limited devices. For example, the extra semiconductor can be used to provide field programmable gate array (FPGA) functionality, test circuitry or to increase device density. Devices are also available that use the extra space to incorporate random access memory (RAM) into each cell. The RAM can then be used to program look-up-tables (LUT's) in the cells. If a particular cell's logic is to be unused, the RAM in that cell can be used as a stand-alone, general purpose RAM device, which can alleviate the need to add a block of RAM to the chip as shown in

FIG. 1. However, the RAM in the cell of such a device cannot be used simultaneously with the gate array logic in the cell.

SUMMARY

[0006] The present invention provides for the incorporation of RAM into the logic array in a distributed fashion, so that a single cell fabric can provide both logic and RAM functionality simultaneously while substantially maximizing the amount of configurable metal for routing. The extra semiconductor area in the cells of a metal limited device is used to implement general purpose RAM that never needs to be used to configure the logic. Common select lines and read/write lines for the RAM are embedded in the base cells so that the configurable metal (whether via or actual metal layer) over the RAM can be used for routing logic.

[0007] According to at least some embodiments of the invention, a mask-configurable semiconductor chip is built to be finished by providing masks to be used in routing metal layers on top of the chip. The chip has an array of logic cells, and at least some logic cells in the array comprise both mask-configurable gate array logic, and random access memory (RAM). The RAM in each of those cells is connected to common select and read/write lines to form distributed RAM so that the RAM is usable simultaneously with the mask-configurable gate array logic.

[0008] In some embodiments, the chip is designed to be configured (customized) using less than the actual number of metal (including via) layer masks that will actually be used to create a final device. In some cases, this configuration

will be accomplished with a single metal layer mask, which may be either a mask designed to create a layer of actual metal traces, or a layer of vias which move signals between metal layers.

[0009] In any case, a completed device is made by first forming the semiconductor layer where cells contain both mask-configurable gate array logic and random access memory (RAM) as described above. Then, the plurality of metal layers are formed top of the semiconductor layer for routing connections. At least some of the plurality of metal layers are customized and are used to configure the device for a specific application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 illustrates a prior art gate array device that also incorporates a block of RAM.

[0011] FIG. 2 illustrates the semiconductor layer of a prior art, metal limited device.

[0012] FIG. 3 illustrates a distributed RAM architecture according to at least some embodiments of the present invention.

[0013] FIG. 4 illustrates both the structure of and method of making a semiconductor layer and a finished device according to the present invention.

[0014] FIG. 5 is a logic diagram for a cell of one of many possible gate array architectures that can be used with the invention.

[0015] FIG. 6 illustrates the gate array architecture that encompasses the logic shown in FIG. 5.

DETAILED DESCRIPTION OF ONE OR MORE EMBODIMENTS

[0016] The present invention will now be described in terms of specific, example embodiments. It is to be understood that the invention is not limited to the example embodiments disclosed. The meaning of certain terms as used in the context of this disclosure should be understood as follows. The term "configuration" and variants such as "configurable" and "configured" refer to the property or process of imparting application-specific function to an integrated circuit chip. The term "metal layer" refers to any layers which are used to make connections to implement the functions of the cells of a device. These metal layers may be the same for every version of a semiconductor device, or they may be used for configuration. In addition, metal layers may contain actual metal routing traces or vias, which provide vertical connectivity between metal routing layers. Finally, the term "chip" and variations such as "integrated circuit chip" or "semiconductor chip" are normally meant to refer to an intermediate device which has not been configured, and may be in the form of a wafer. A finished device such as an application-specific integrated circuit (ASIC) will be referred to as a "device" or with a variant term such as "semiconductor device" or the like. Other terms will either be discussed when introduced, or otherwise should be assumed to have the conventional meaning as understood by persons of ordinary skill in the art.

[0017] FIG. 3 is a conceptual, block diagram of a distributed RAM architecture, which is used to implement example embodiments of the invention. The distributed RAM of FIG. 3 consists of multiple, medium sized dual port RAM blocks 301. Not every block of RAM in FIG. 3 is labeled as to do so would adversely effect the clarity of the diagram. In this example, each block of RAM contains 8 by 1 bits. In an actual device, general purpose logic can be added to allow the combination of multiple medium size RAM blocks into larger arrays of RAM. However, a dual port RAM of medium size will satisfy most needs. Additionally, if only a smaller amount of RAM than this is needed, the amount of semiconductor wasted will still be relatively small.

[0018] Returning to FIG. 3, address decoders 302 contain the appropriate number of inputs for the chosen RAM architecture. The select lines for the address decoders are common to multiple blocks of RAM. Of course, multiple select lines are present. Only one select line, 304, is shown for clarity. Likewise, read/write logic 306 drives an appropriate number of read/write lines for the specific RAM architecture and size chosen. Data lines from the read/write logic are common to multiple blocks of RAM. Data line 308 is shown for illustrative purposes. Again, multiple data lines are present, but only one is shown for clarity. In the example RAM architecture shown, the select lines are word select lines. Depending on the architecture, select lines could also be address select lines, used to select bits in a column according to an address. In any case, such lines are referred to herein as "select" lines.

[0019] FIG. 4 is a conceptual, block diagram illustrating a chip according to the invention, as well as a device, and the method of making the device according to at

least some embodiments of the present invention. Like reference numbers are used for like structures across Figures 3 and 4 in this disclosure. The device, 400, includes read/write logic 306 and address decoders 302 just as in FIG. 3. The device of FIG. 4 also includes select lines 304 as shown in FIG. 3. The device 400 also includes data lines 308 as shown in FIG. 3. In this case, the RAM blocks are disposed within multiple, substantially identical logic cells 406. Each logic cell 406 contains RAM block 402 and mask configurable gate array logic block 404. It should be noted that the select and data lines for the RAM in the example embodiments are embedded within the semiconductor, for example, polysilicon portion of the chip, or are routed via the non-configurable metal layers. These lines are not routed through the configurable metal layers.

[0020] In one example, 8 by 1 RAM blocks are used in FIG. 3, and each block has eight, one-bit addressable registers. Thus, three select lines are provided per column to enable a word select function for the address decoders. In this case, a single read and single write line are provided per row. Although a specific word select is communicated to multiple RAM blocks, the read/write logic determines which one is actually read or written, as the case may be, in a particular column of distributed RAM. Other memory architectures can be used. In particular however, having word select lines in one direction and data lines in another works well. Word lines are for selecting a column (assuming vertical word lines) of RAM bits to be read or written. The data lines either communicate the data to be written to the selected column (assuming horizontal data lines) or allow data from the selected column to be

transmitted to read/write logic at the edge. A dual-port RAM architecture can be implemented, among other ways, by having two sets of word select and data lines present, one for each port.

[0021] The semiconductor chip shown in FIG. 4 is made into the finished device, 400, by adding multiple metal layers, 408, shown in cutaway, to the semiconductor chip. At least some of the layers impart configuration information to the device. In a practical integrated circuit device, wafers may be held in inventory with no metal layers present, and then all of the metal layers added when a configured device is ordered. This process may be the same even if some of the metal layers are the same from one application specific device to another. It would also be possible to design a system whereby some of the metal layers, which do not impart configuration specific properties to the device, have already been added to the intermediate semiconductor chip.

[0022] Having described a RAM architecture and an overall design for a logic array according to the present invention, some example gate array logic architectures which can be used with the invention will now be discussed. It must be emphasized that the choice of gate array logic cell architectures to be used with the distributed RAM invention described herein is almost infinite. The examples described are provided merely to completely enable some embodiments of the invention and are not intended to limit the scope or spirit of the invention. Ideally, to maintain the advantages of low NRE and quick turn, the gate array logic used in a chip and device according to the invention should be configurable with as few masks as possible.

[0023] U.S. Patent 6,014,038 to How et al. describes a function block architecture which requires minimal masking steps, and is incorporated herein by reference. With the architecture described by How, each function block is generally composed of two computation modules and a communication module, each having fixed internal architecture, but whose functions can be varied by varying input signals to each module. Computation modules are identical mirror images of each other. Each computation module is divided into two stages. One stage contains one multiplexer, and a second stage generally includes three multiplexers.

[0024] U.S. Patent 6,294,927 to Yoeli et al. describes a configurable cell architecture for a customizable logic array device, and is incorporated herein by reference. The architecture of Yoeli requires either a single metal trace layer, or a metal trace layer and a via layer for configuration. Each logic unit includes multiplexers, a NAND gate, and an inverter. Alternative architectures are discussed, however, simplicity is a particular feature of the cells described.

[0025] Another logic cell architecture that can be used with the invention is described in U.S. Patent 6,331,790 to Or-bach et al., which is incorporated herein by reference. Still another cell architecture which could work with the invention is described in U.S. Patent 5, 068,603 to Mahoney, which is also incorporated herein by reference. Still another cell architecture which can be used with the present invention is described in Figures 5 and 6 of the present disclosure.

[0026] FIG. 5 is a detailed logic diagram of one of the cells of an architecture, which can be configured with a single via mask. The cell, 500, includes three look-up

tables (LUT's). The LUT inputs are shown at 501. LUT 502 is a three logic input LUT. LUT 504 is a three logic input LUT. LUT 506 has two logic inputs. There is routing internal to the cell to allow any LUT to drive at least one input on any other LUT. Any LUT can also drive the D input of flip-flop 508. The configuration can be controlled in part by selecting via connections at positions illustrated as shown at 509. The cell also includes two inverters 510, which can instead be buffers. The inverters or buffers serve to increase drive strength. Jumpers J1, J2, J3 and J4 can provide an increase in density by allowing some configuration of this portion of the cell outside of using the configurable metal layers.

[0027] A LUT, as shown in FIG. 5, is built from one or more multiplexers with constant data inputs. The logic inputs drive the select lines of the multiplexers (not to be confused with select lines for the RAM as previously discussed). A LUT of N inputs can be implemented with a multiplexer of 2^n data inputs programmably tied to one of the supply voltages through vias. In a practical semiconductor device, each LUT can be provided with appropriate test data lines to carry data from a selected column of the LUT to the edge of the chip die for testing. Of course, in such a case lines are also provided to determine which column's data is to be communicated to the edge. The lines associated with this testing are omitted from FIG. 5 for clarity.

[0028] FIG. 6 illustrates how cell logic 500 of FIG. 5 is connected to other logic cells in an actual device. LUT inputs 501 are again shown in FIG. 6. Vias are illustrated as shown at 601. Lines to gate array logic blocks in adjacent cells are also shown. Inputs, which are connected to outputs of the logic cell where the

connections cannot be shown directly for clarity, are labeled appropriately. The reset and clock lines which are shown connected to flip-flop 508 of FIG. 5 are also labeled in FIG. 6.

[0029] With the architecture shown in Figures 5 and 6, an 8 by 8 array of logic cells would have 64 connection pads. The exact clocking and reset scheme would depend on the implementation, however, in one embodiment, there is a clock and reset signal generator every eight rows of logic cells. Additional information on the via layer programmed architecture described immediately above can be found in U.S. Patent application 60/296,854, filed June 8, 2001, which is incorporated herein by reference.

[0030] Specific embodiments of an invention are described herein. One of ordinary skill in the semiconductor arts will quickly recognize that the invention has other applications in other environments. In fact, many embodiments and implementations are possible. The following claims are in no way intended to limit the scope of the invention to the specific embodiments described above. I claim:

CLAIMS

1. A mask-configurable semiconductor chip comprising an array of logic cells, wherein at least some logic cells in the array comprise:

mask-configurable gate array logic; and

random access memory (RAM), wherein the RAM in each of the at least some logic cells is connected to common select and read/write lines to form distributed RAM so that the RAM is usable simultaneously with the mask-configurable gate array logic.

2. The mask-configurable semiconductor chip of claim 1 wherein the gate array logic is arranged to be substantially configured with a single layer mask.

3. The mask-configurable semiconductor chip of claim 2 wherein the single layer mask is a via mask for producing a via layer.

4. A semiconductor device comprising:

a semiconductor layer further comprising:

mask-configurable gate array logic; and

random access memory (RAM), wherein the RAM in each of the at least some logic cells is connected to common select and read/write lines to form distributed RAM so that the RAM is usable simultaneously with the mask-configurable gate array logic; and

a plurality of metal layers disposed an top of the semiconductor layer for routing connections wherein at least some of the plurality of metal layers configures the gate array logic.

5. The semiconductor device of claim 4 wherein the gate array logic is configured with only some of the plurality of metal layers.

6. The semiconductor device of claim 4 wherein the gate array logic is substantially configured with only one of the plurality of metal layers.

7. The semiconductor device of claim 6 wherein the one of the plurality of metal layers is a via layer.

8. A method of making a semiconductor device comprising the steps of:

forming a semiconductor layer comprising mask-configurable gate array logic and random access memory (RAM), wherein the RAM in each of the at least some logic cells is connected to common select and read/write lines to form distributed RAM so that the RAM is usable simultaneously with the mask-configurable gate array logic; and

forming a plurality of metal layers disposed an top of the semiconductor layer for routing connections wherein at least some of the plurality of metal layers configures the gate array logic.

9. The method of claim 8 wherein the gate array logic is configured with only some of the plurality of metal layers.

10. The method of claim 8 wherein the gate array logic is substantially configured with only one of the plurality of metal layers.

11. The method of claim 10 wherein the one of the plurality of metal layers is a via layer.

ABSTRACT OF THE DISCLOSURE

Distributed RAM in a logic array. A single, customizable, logic array fabric provides both gate array logic and RAM functionality simultaneously while substantially maximizing the amount of configurable metal for routing. The extra semiconductor area in the cells of a metal limited device is used to implement general purpose RAM. Common select lines and read/write lines for the RAM are embedded in the base cells so that the configurable metal (whether via or actual metal layer) over the RAM can be used for routing logic.

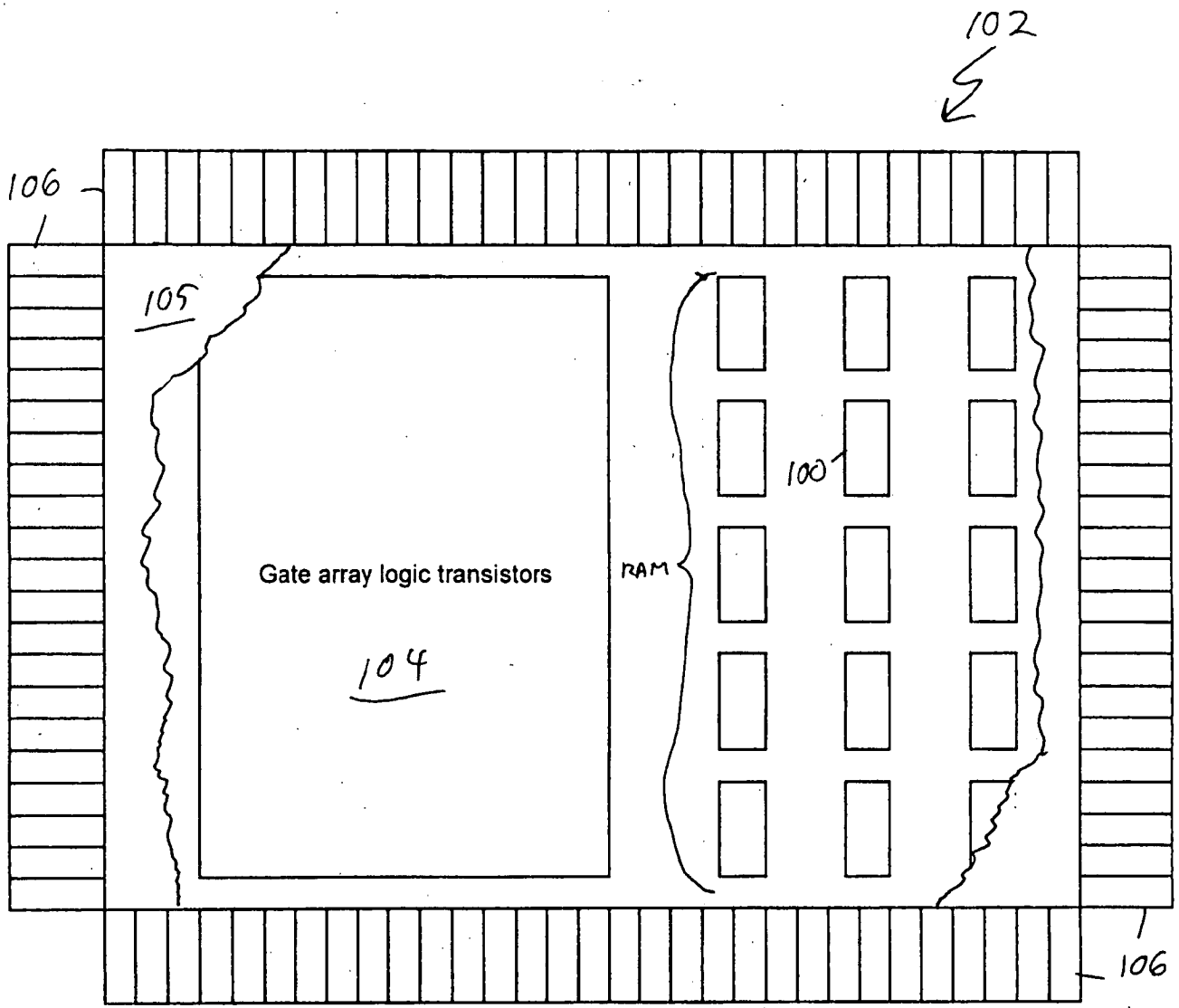


FIG. 1
(PRIOR ART)

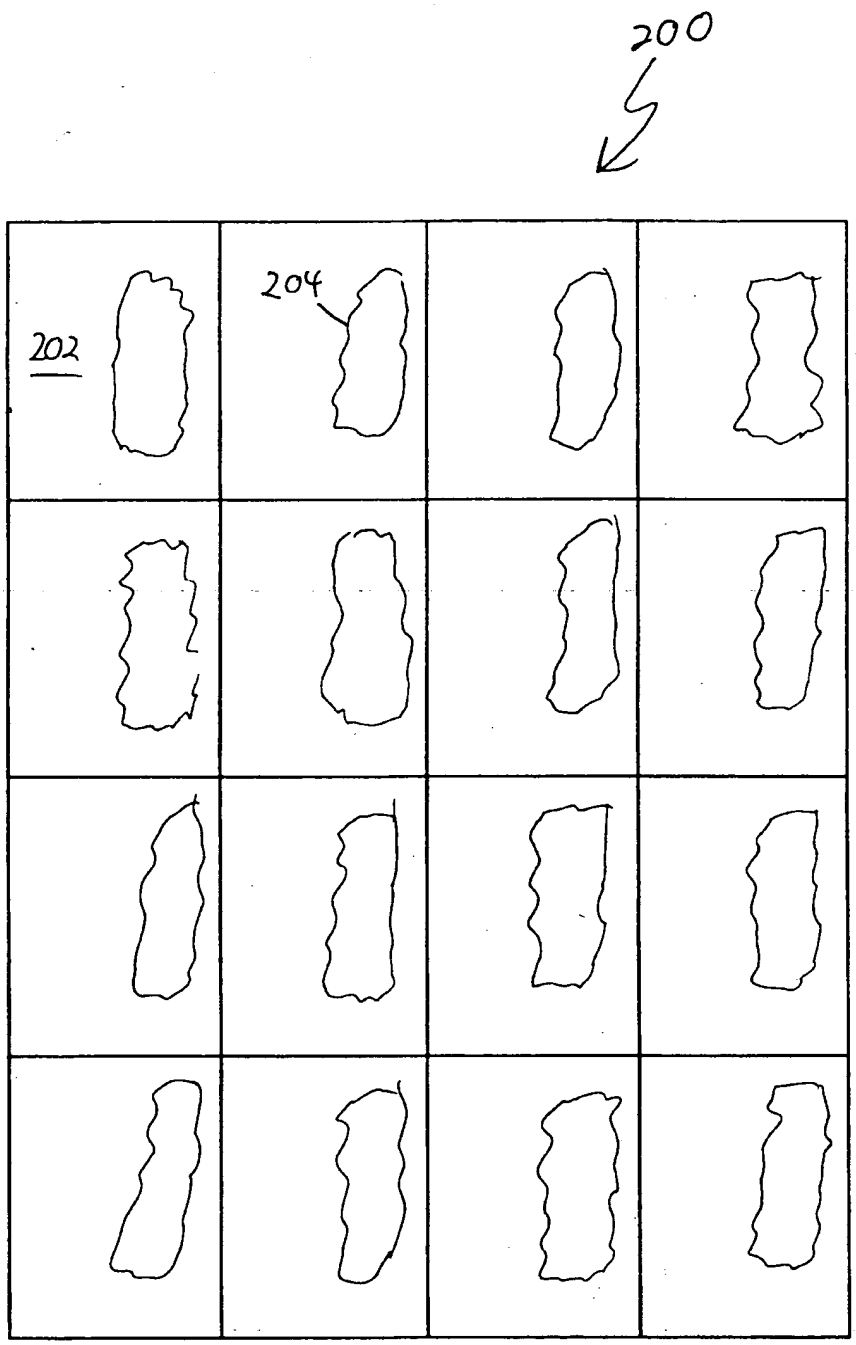


FIG. 2
(PRIOR ART)

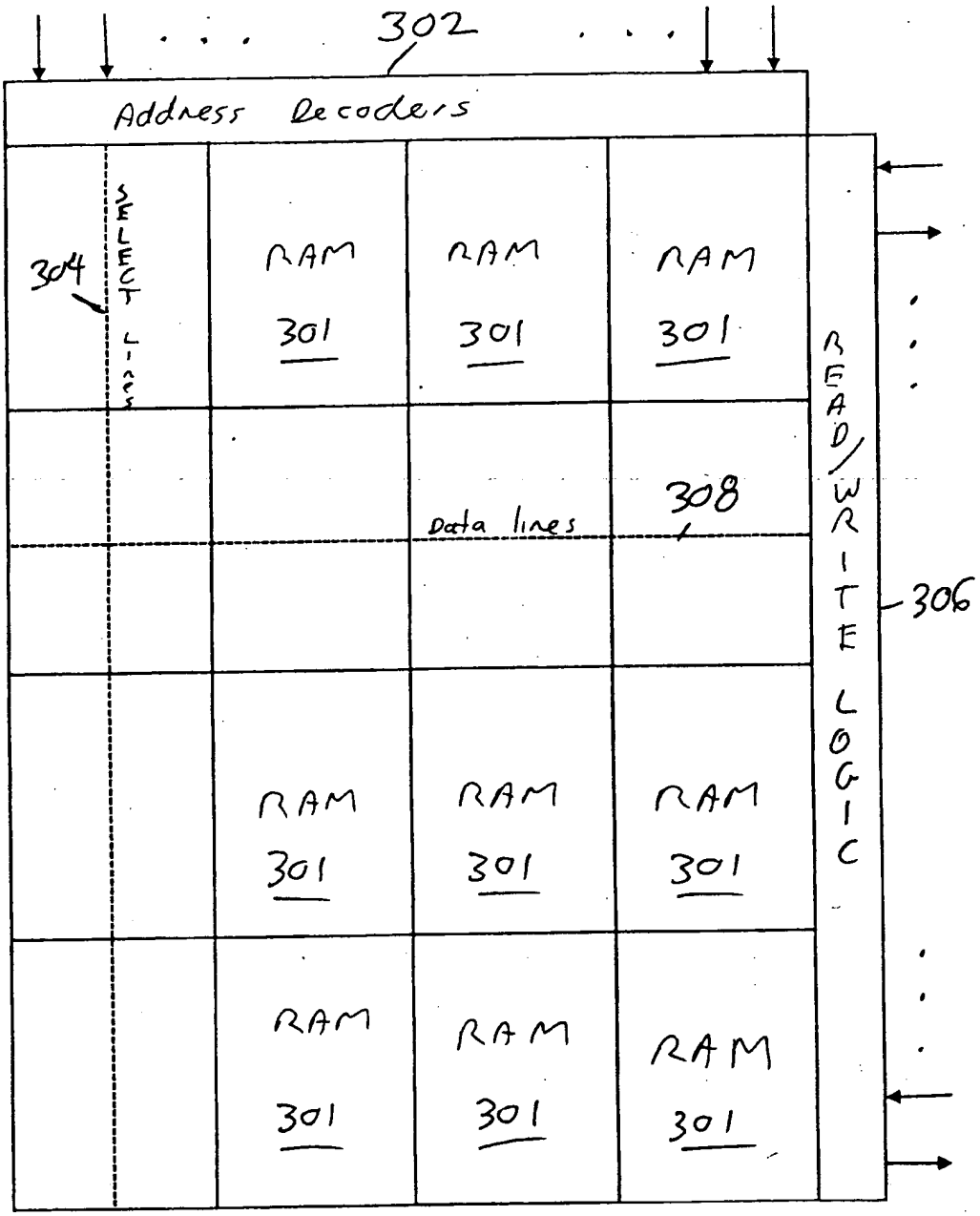

302
Address Decoders
304
SELECT LINES
RAM 301
data lines
308
READ/WRITE LOGIC
306

FIG. 3

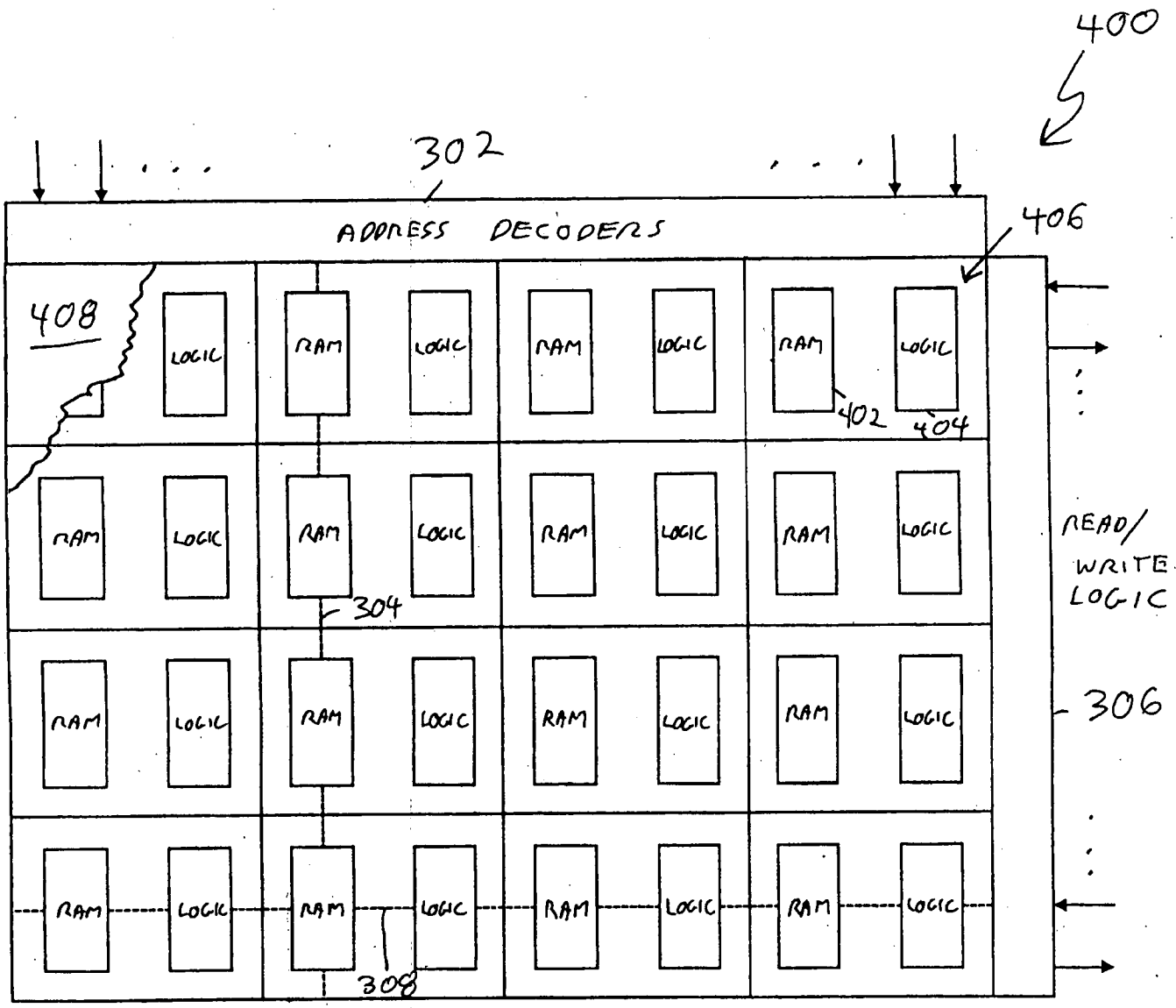
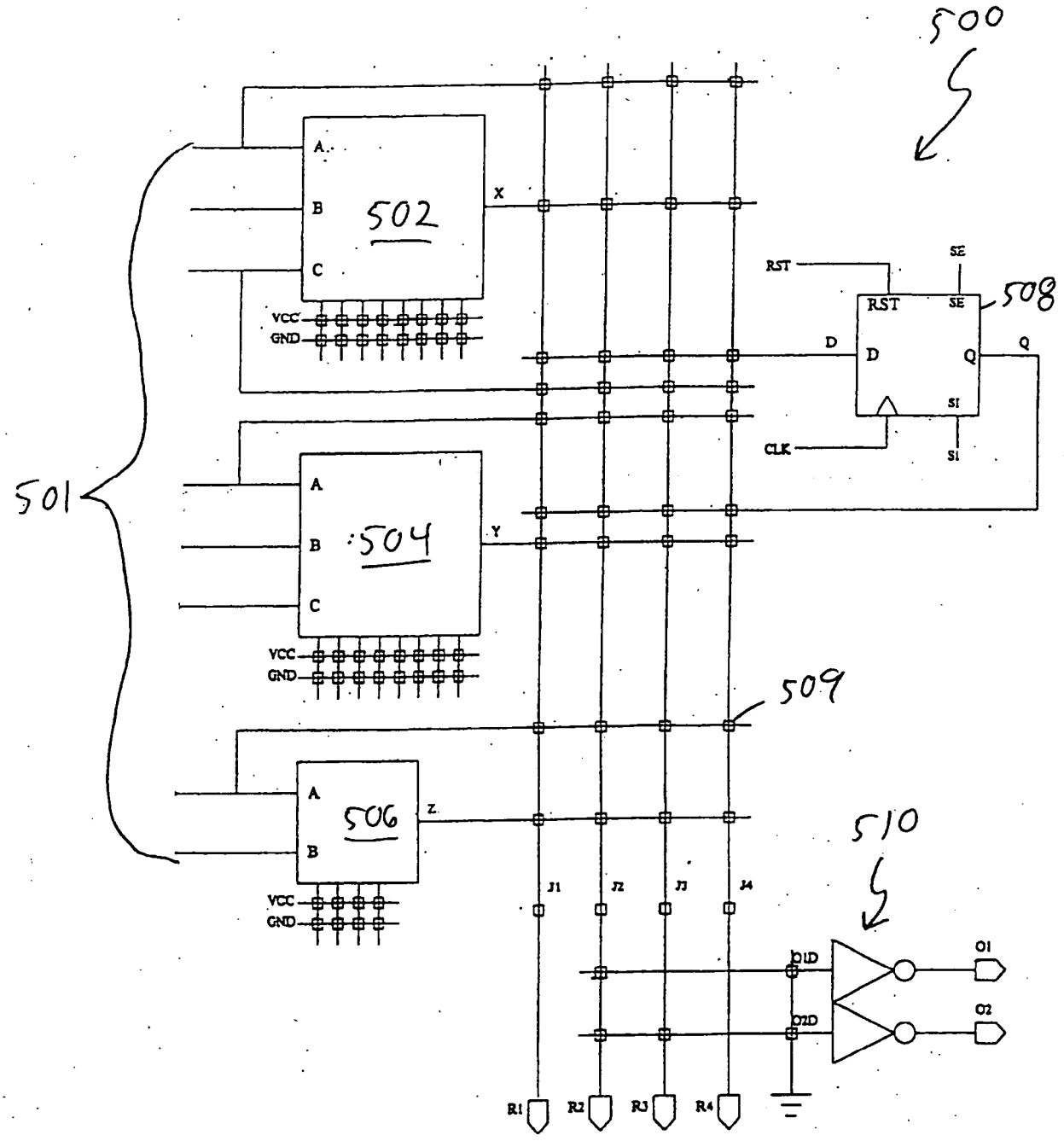

400
302
ADDRESS DECODERS
406
408
LOGIC
RAM
402
404
304
READ/
WRITE
LOGIC
306
308

FIG. 4


500
502
504
506
501
509
510
508
A
B
C
X
Y
Z
VCC
GND
RST
SE
D
Q
SI
CLK
J1
J2
J3
J4
R1
R2
R3
R4
O1D
O2D
O1
O2

F16.5

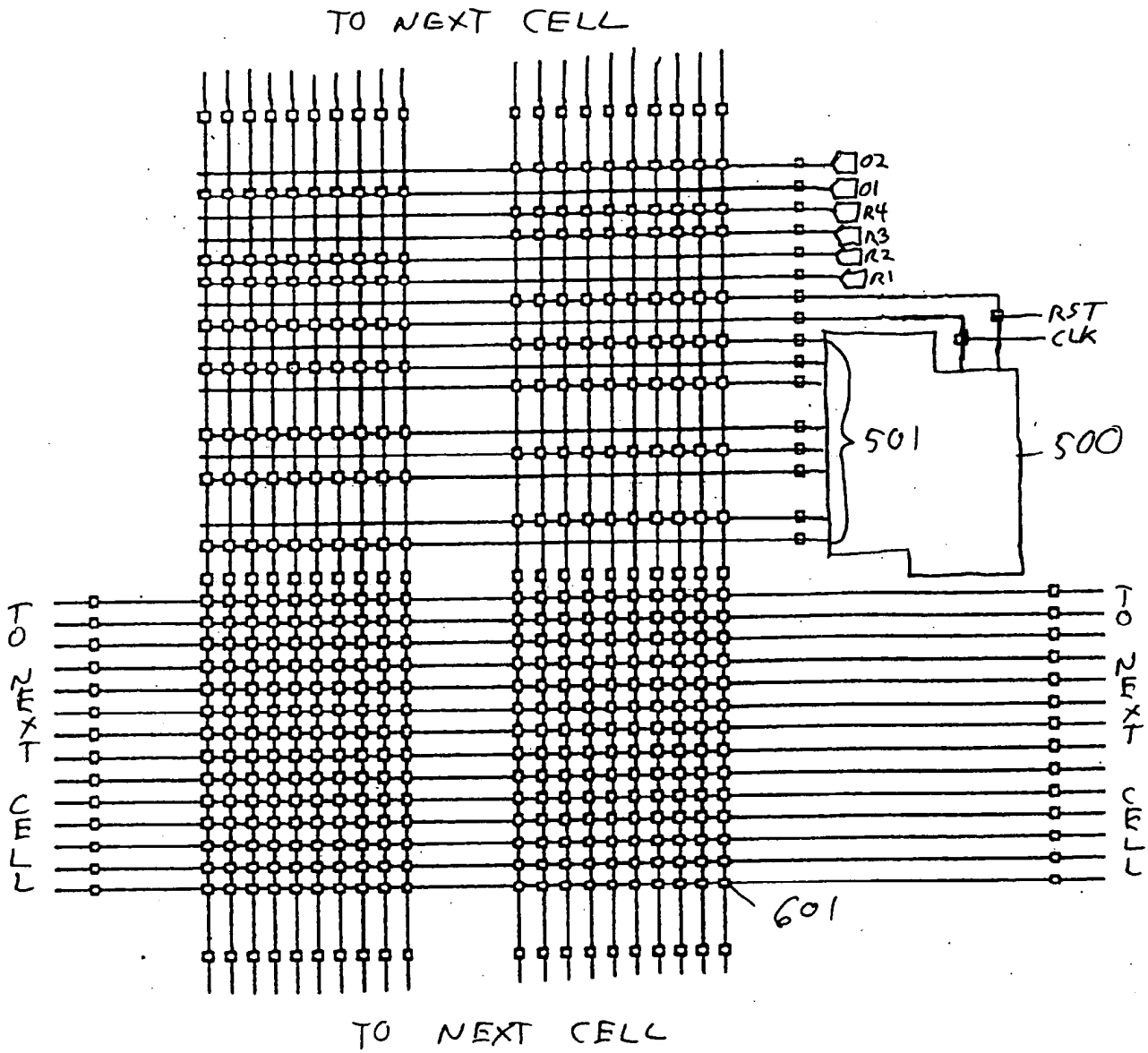

TO NEXT CELL
O2
O1
R4
R3
R2
R1
RST
CLK
501
500
TO NEXT CELL
TO NEXT CELL
601
TO NEXT CELL

FIG. 6

FIG. 1

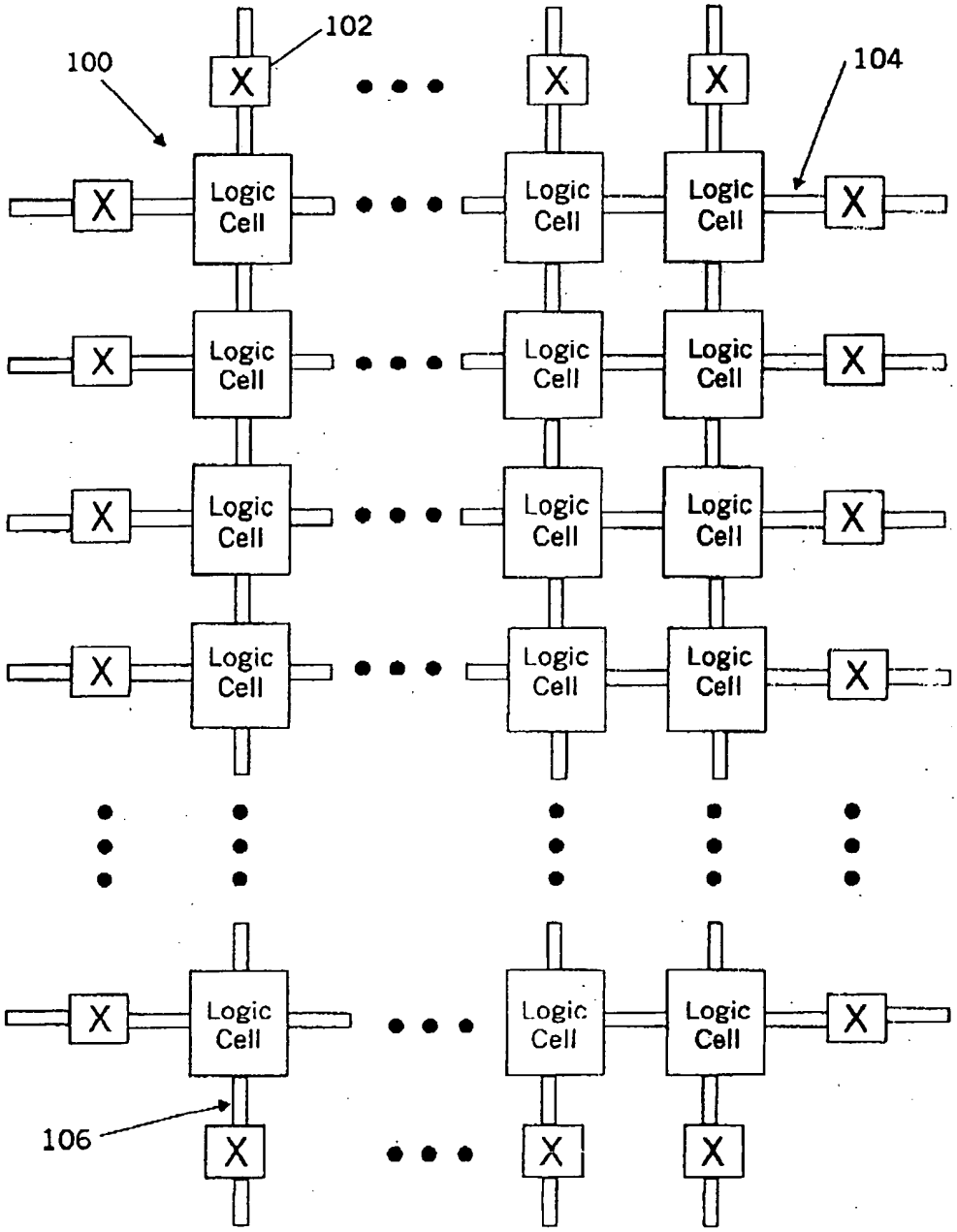


FIG. 2

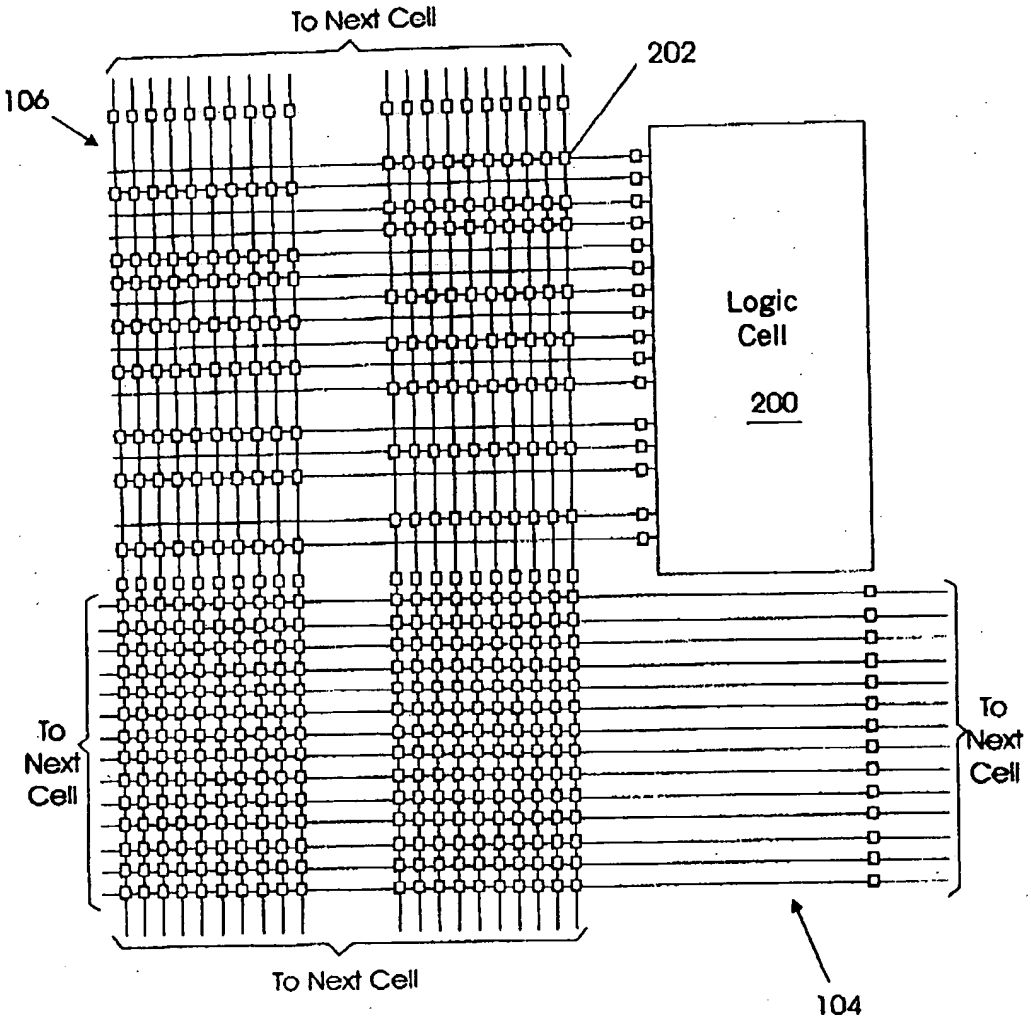

To Next Cell
202
106
Logic
Cell
200
To
Next
Cell
To
Next
Cell
To Next Cell
104

FIG. 3

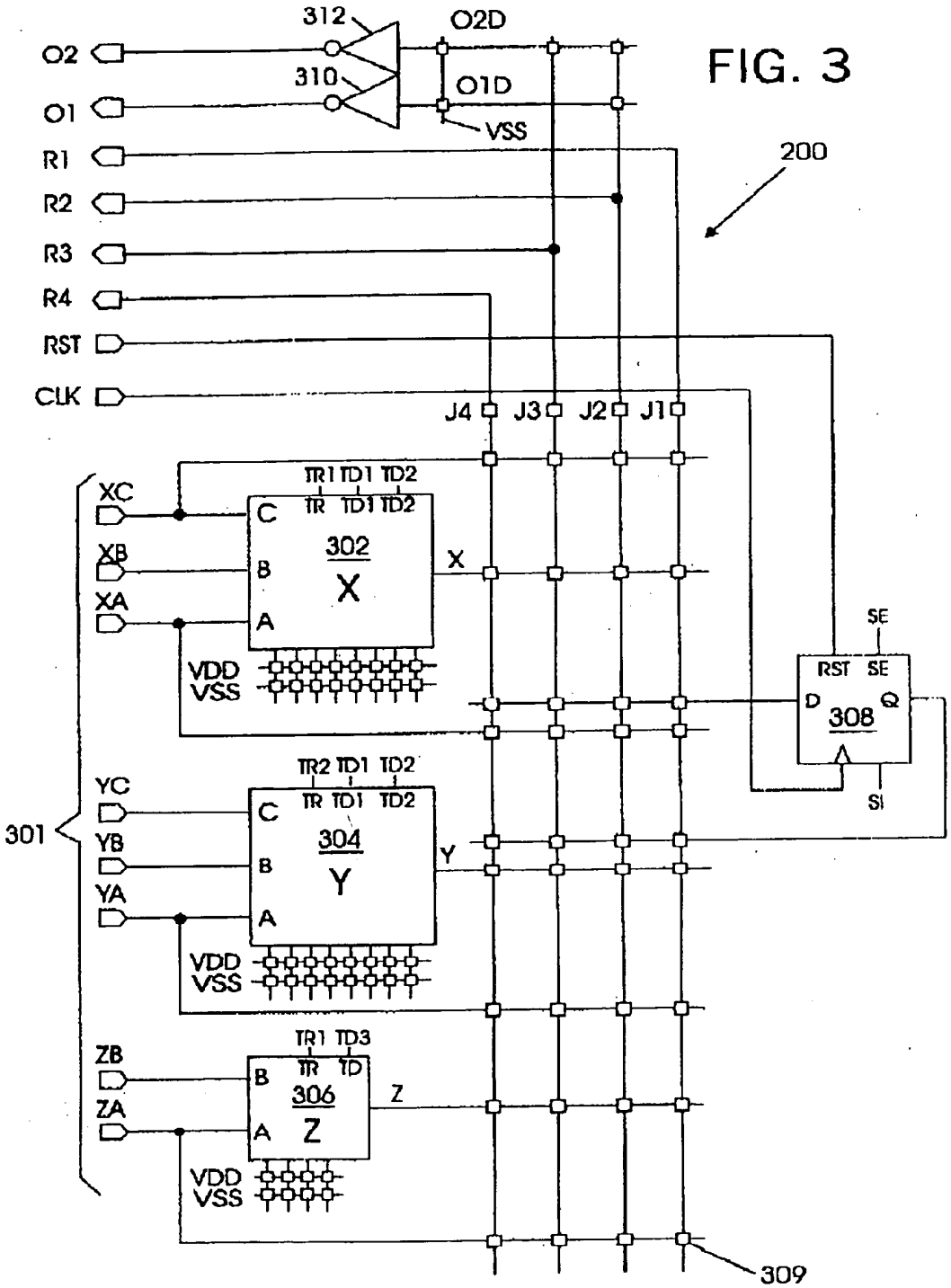

312
O2D
O2
310
O1D
O1
VSS
R1
R2
R3
R4
RST
CLK
200
J4 J3 J2 J1
TR1 TD1 TD2
XC
C
TR TD1 TD2
302
XB
B
X
XA
A
VDD
VSS
SE
RST SE
D
Q
308
SI
TR2 TD1 TD2
YC
C
TR TD1 TD2
301
304
YB
B
Y
YA
A
VDD
VSS
TR1 TD3
ZB
B
TR TD
306
Z
ZA
A
Z
VDD
VSS
309

FIG. 4

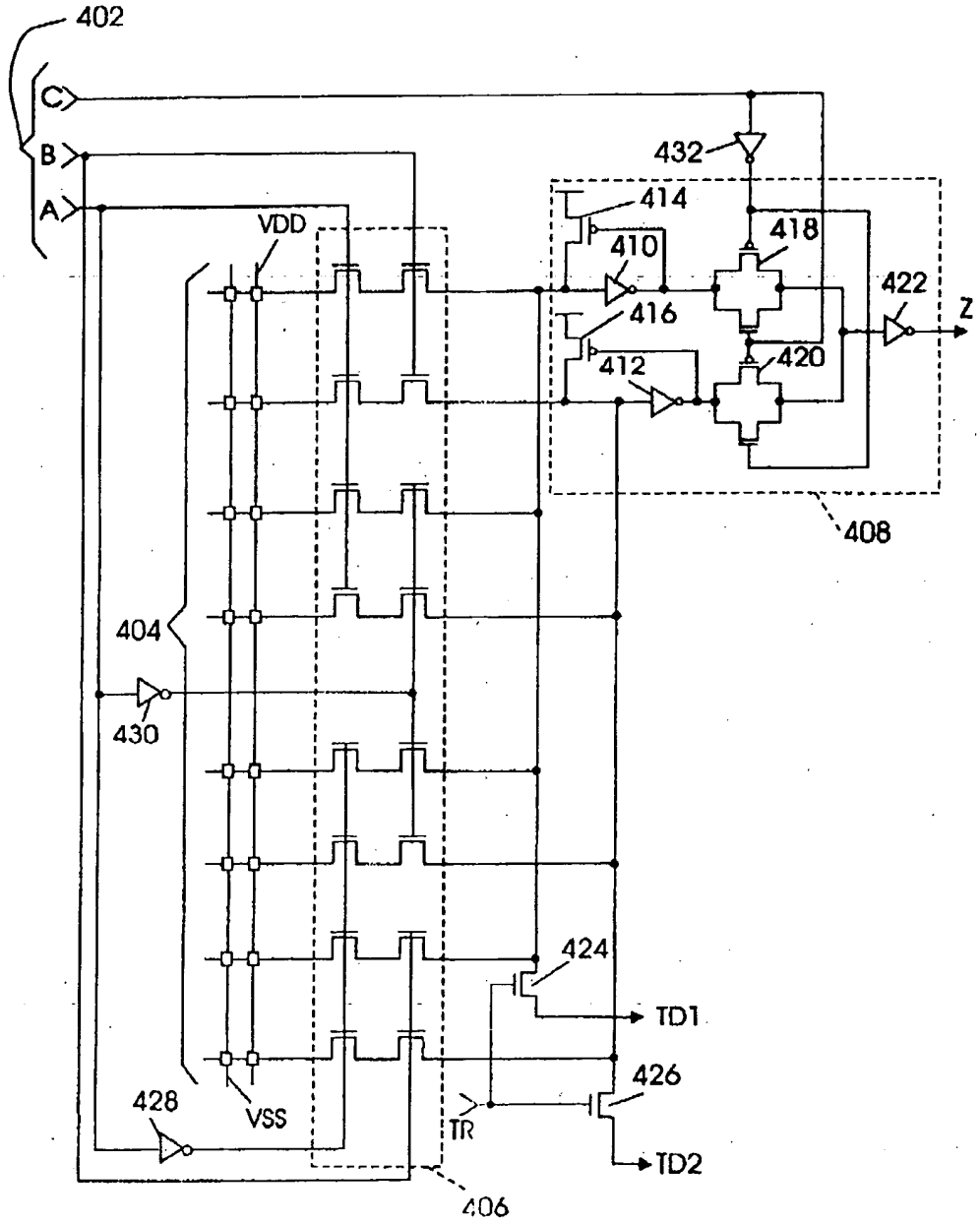

402
C
B
A
VDD
VSS
404
430
428
432
414
410
416
412
418
420
422
Z
408
424
TD1
426
TR
TD2
406

FIG. 5

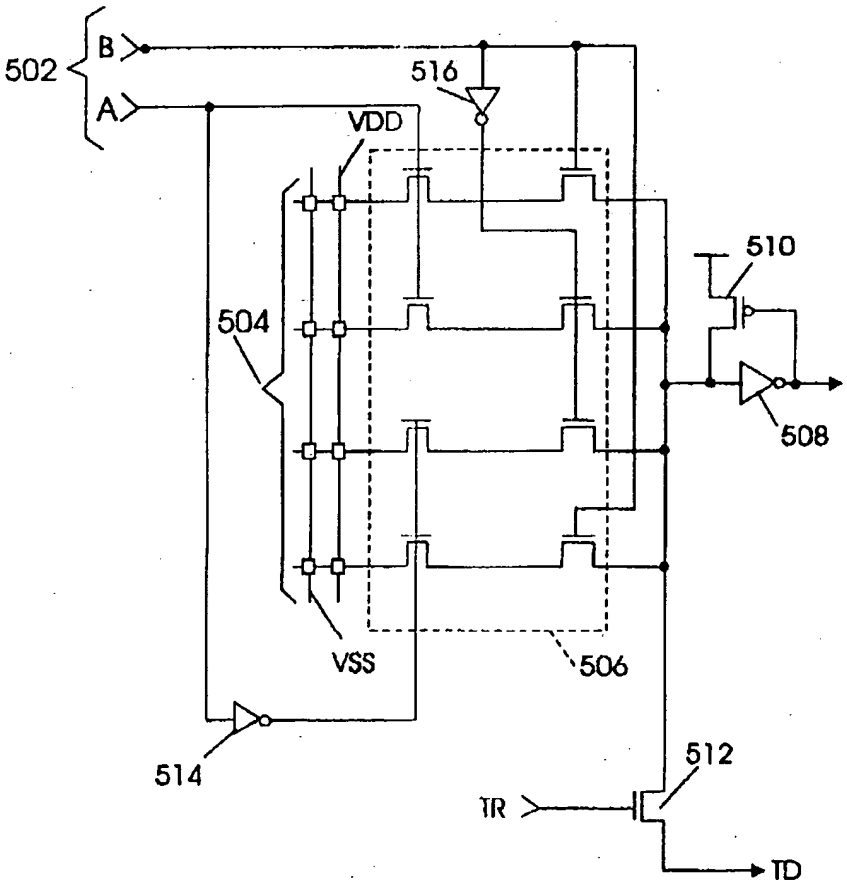


FIG. 6

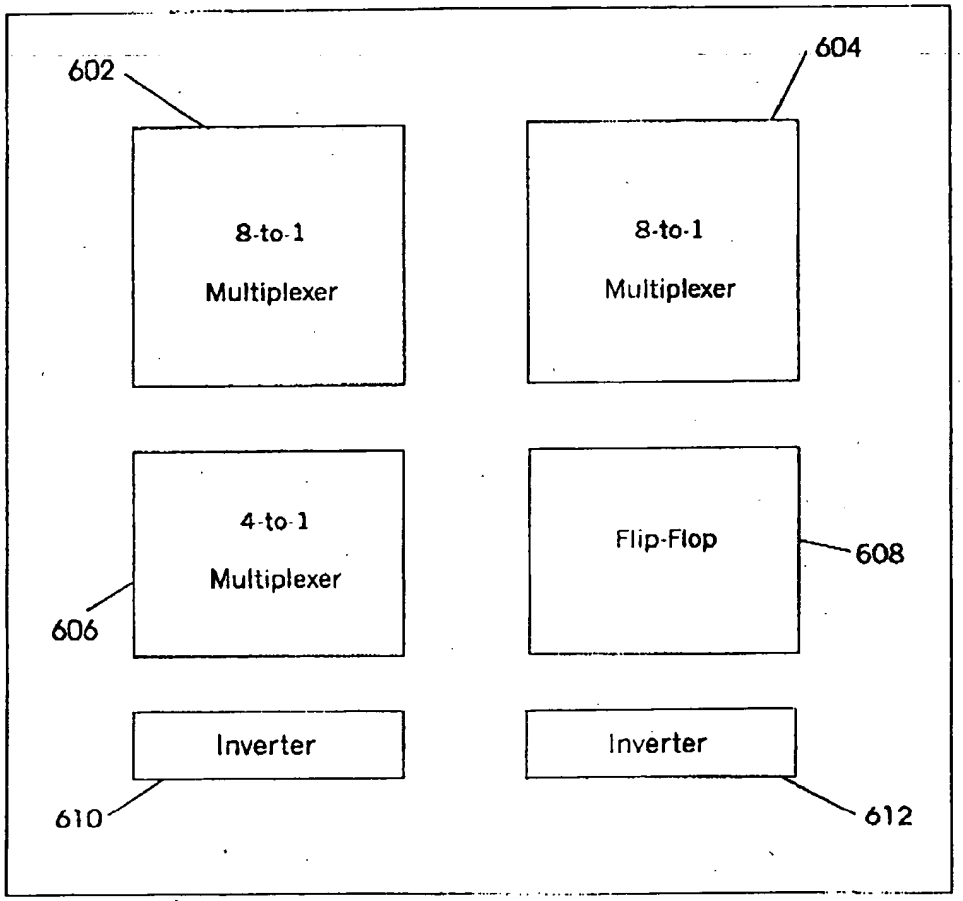

602
604
8-to-1
Multiplexer
8-to-1
Multiplexer
4-to-1
Multiplexer
606
Flip-Flop
608
Inverter
Inverter
610
612

FIG. 7

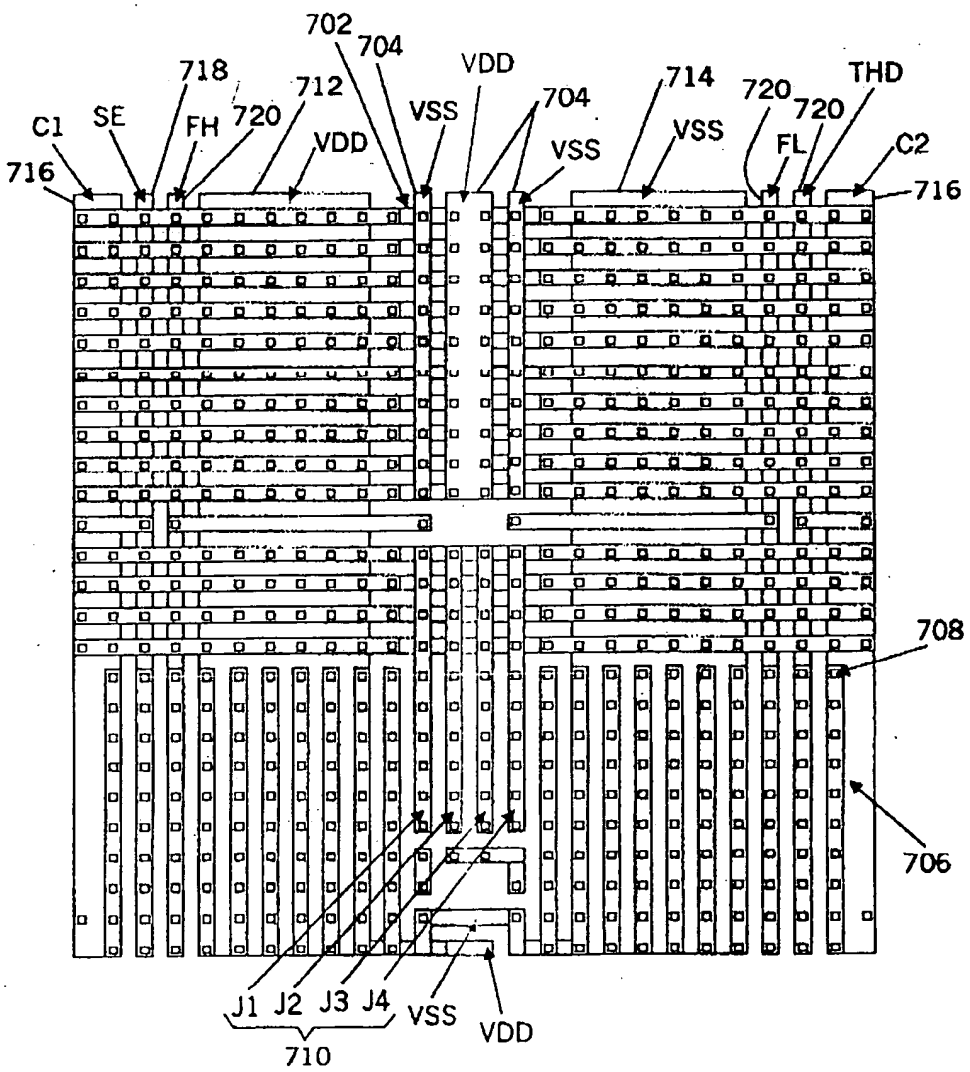

702
704
718
712
VDD
714
720
THD
C1
SE
FH
720
VSS
704
VSS
720
FL
C2
716
VDD
VSS
716
708
706
J1 J2 J3 J4
VSS
VDD
710

FIG. 8

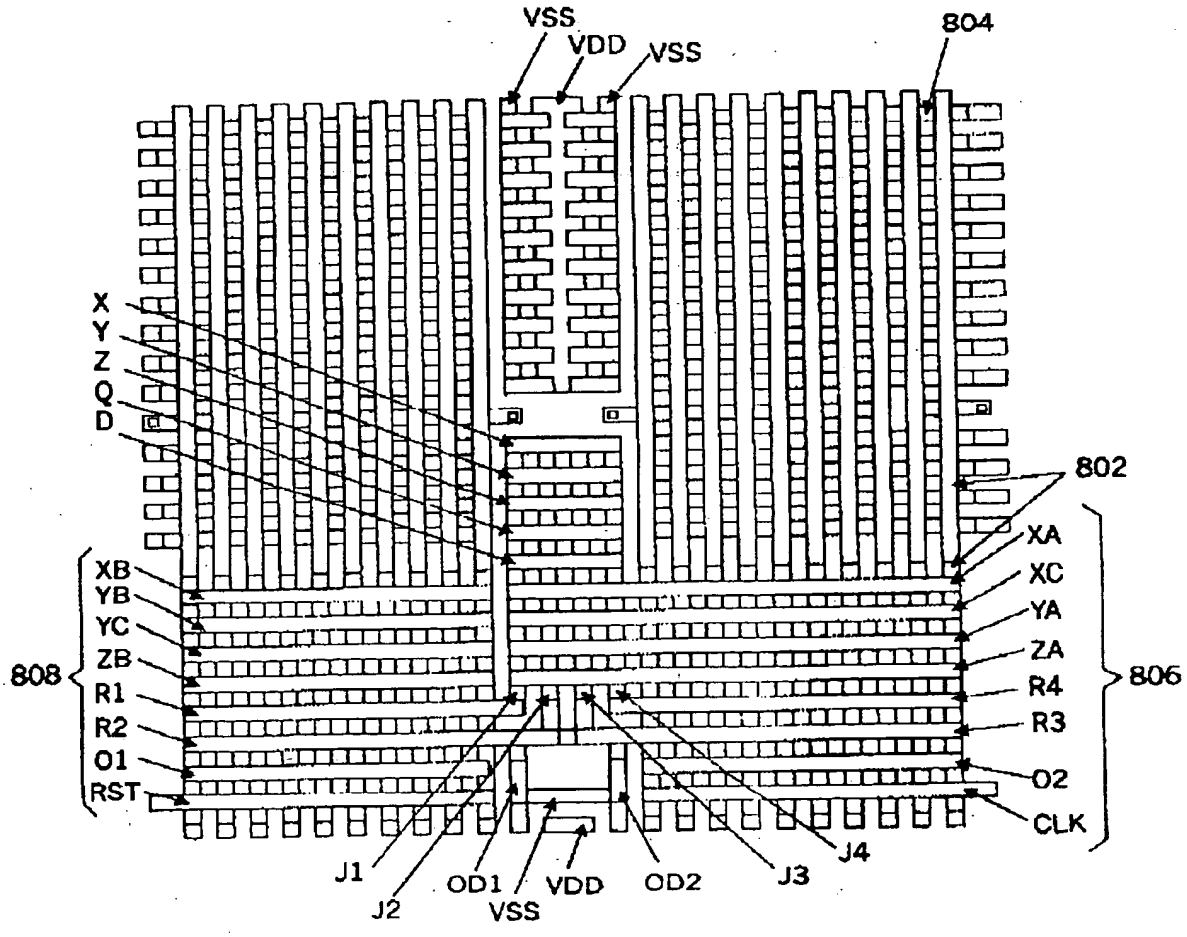
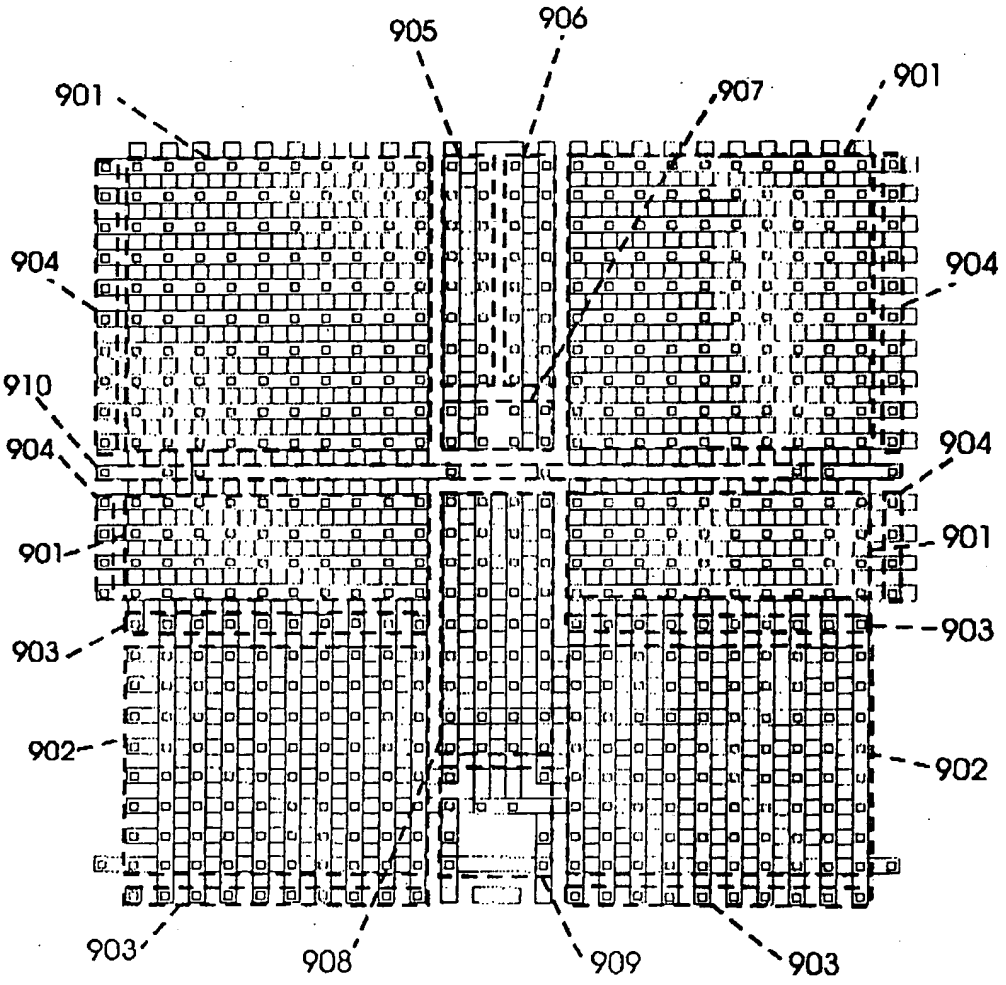

VSS
VDD
VSS
804
X
Y
Z
Q
D
802
XA
XC
YA
ZA
R4
R3
O2
CLK
806
XB
YB
YC
ZB
R1
R2
O1
RST
808
J1
J2
OD1
VSS
VDD
OD2
J3
J4

FIG. 9


905
906
907
901
901
904
904
910
904
904
901
901
903
903
902
902
903
908
909
903

CELL ARCHITECTURE TO REDUCE CUSTOMIZATION IN A SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from co-pending provisional patent application serial number 60/296,854, filed June 8, 2001, by the inventor hereof, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] For many years, gate arrays have been used to provide quick-turnaround, low non-recurring-expense (NRE) semiconductor devices that are used for a variety of purposes. Traditionally, semiconductor wafers are processed up to but not including the first (bottom) metal layer, and then the wafers are saved in inventory. When a customer orders a semiconductor device to be fabricated for a specific application (an application specific integrated circuit or "ASIC"), the customer only has to pay for the masks that are required to configure the metal layers, but not for the transistor layers below. Thus, NRE is reduced. The wafers may be completed quickly, since only the metal layers remain to be fabricated, which also reduces the turn-around time that is necessary to build the device.

[0003] Recently more and more layers of metal have been incorporated into gate array semiconductor devices. Rather than two or three layers of metal, six to eight layers of metal are now common. As a result, gate arrays

are no longer very low NRE, or provide quick-turnaround times. In order to regain the advantages of earlier gate arrays, several vendors have developed logic arrays, consisting of multiple, substantially identical logic cells, that may be configured for an application with either fewer or cheaper masks. In the case of fewer masks, the total number of metal layers and hence masks used to create the finished device often does not change. Rather, only a reduced subset of the total number of metal layers in a finished device are used to impart the custom configuration to the device. For example, so-called "one-mask" devices, in which only a single metal layer and hence a single mask imparts customization, may reduce both NRE and the turnaround-time.

[0004] An ASIC is a semiconductor device that combines large numbers of programmable blocks of logic circuits into a logic cell to create a device that is specifically adapted for a particular application, but at a cost that is lower than that of developing a completely new device from scratch. Like most integrated circuit chips, ASIC chips are manufactured using a lithographic process that depends on having a mask for each layer of the chip. In the case of a completely new chip, many unique masks may be required. In the case of an ASIC such as a gate array, however, some masks are generic, that is, the same for each different type of ASIC of a given programmable architecture, regardless of the application, while some are custom. It is the custom masks that impart the application specificity to the chip by programming the logic cells during the manufacturing process. Multiple custom masks may be required to

accomplish the programming of an ASIC. The number depends to some extent on the design of the programmable cells. Although the number of custom masks required is less than the total number of masks, and certainly less than the number of masks required to create a completely new chip from scratch, each custom mask represents a significant cost in both money and development time.

[0005] In many cases, the cell architecture of an ASIC may be designed to reduce the number of custom masks that may be required to just one mask, which provides a significant cost and time savings. A "one mask" device allows all of the masks to remain generic except for a single mask, thus allowing the semiconductor manufacturer to invest in the generic or base masks just one time. Various designs may be implemented by customizing just a single mask instead of a complete mask set.

SUMMARY

[0006] The present invention provides for a semiconductor device and a method of testing the device having a plurality of logic cells interconnected using vias to connect routing tracks that are disposed among a plurality of layers in the device. The logic cells in the device include at least two three-input look-up tables, one two-input look-up table and a flip-flop. The components in the logic cell are connected so that any look-up table can drive at least one input of any other look-up table and where the flip-flop is

connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

[0007] In some embodiments, the semiconductor device may be designed to be configured or customized using less than the actual number of metal (including via) layer masks that will actually be used to create a final device. In some cases, this configuration will be accomplished with a single metal layer mask, which may be either a mask designed to create a layer of actual metal traces, or a layer of vias which move signals between metal layers.

[0008] In any case, a completed device is made by first forming the semiconductor layer where cells contain mask-configurable gate array as described above. Then, the plurality of metal layers are formed on top of the semiconductor layer for routing connections. At least some of the plurality of metal layers are customized and may be used to configure the device for a specific application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 illustrates an 8 by 8 array of logic cells according to at least some embodiments of the present invention.

[0010] FIG. 2 illustrates a single logic cell and surrounding routing tracks according to the present invention.

[0011] FIG. 3 is a detailed logic diagram of a single cell architecture that may be used with the invention.

[0012] FIG. 4 illustrates an exemplary 3-input lookup table with a test circuit according to at least some embodiments of the present invention.

[0013] FIG. 5 illustrates an exemplary 2-input lookup table with a test circuit according to at least some embodiments of the present invention.

[0014] FIG. 6 illustrates an example layout of the logic elements of the cell shown in FIG. 3.

[0015] FIG. 7 illustrates the metal 4 and 5 layers of a typical ASIC using the present invention.

[0016] FIG. 8 illustrates the metal 3 and 4 layers of a typical ASIC using the present invention.

[0017] FIG. 9 illustrates the metal 3 and 4 layers of a typical ASIC with annotations to identify groups of programming vias according to at least some embodiments of the present invention.

DESCRIPTION OF THE INVENTION

[0018] It is to be understood that the present invention is not limited to the example embodiments disclosed herein. The meaning of certain terms as used in the context of this disclosure should be understood as follows. The term "configuration" and variants such as "configurable" and "configured" refer to the property or process of imparting application-specific function to an integrated circuit chip. The term "metal layer" refers to any layers that are used to make connections to implement the functions of the cells of a device.

These metal layers may be the same for every version of a semiconductor device, or they may be used for configuration. In addition, metal layers may contain actual metal routing traces or vias, which provide vertical connectivity between metal routing layers. Finally, the term "chip" and variations such as "integrated circuit chip" or "semiconductor chip" are normally meant to refer to an intermediate device that has not been configured, and may be in the form of a wafer. A finished device such as an application-specific integrated circuit (ASIC) will be referred to as a "device" or with a variant term such as "semiconductor device" or the like. Other terms will either be discussed when introduced, or otherwise should be assumed to have the conventional meaning as understood by persons of ordinary skill in the art.

[0019] The present invention in some embodiments defines a cell architecture for an ASIC that reduces the number of custom masks required to just one mask, representing significant cost and time savings. In some embodiments, the invention allows all of the masks to remain generic except for the via mask, which determines where the so-called "vias" will be placed to make connections between layers. By using the architecture of the invention, the semiconductor manufacturer may invest in the generic or base masks just one time. Various designs are then implemented by customizing just the via mask instead of a complete mask set.

[0020] A device according to the present invention has rows and columns of logic cells, where each cell may implement about 10 ASIC gates worth of

logic. FIG. 1 illustrates an 8 by 8 array of logic cells 100 that would have 32 pads 102 around the edge of the die. Horizontal routing tracks 104 and vertical routing tracks 106 connect the logic cells 100 together. These tracks are formed of segmented wires of fixed length that may be connected end-to-end through vias, which are shown in more detail in FIG. 2. The inputs and outputs of the logic cells 100 communicate using routing tracks 104 and 106 through the vias.

[0021] FIG. 2 illustrates a single logic cell 200 and how the cell connects to surrounding cells. The logic cell 200 is connected to the other logic cells in the array using the horizontal and vertical routing tracks 104 and 106 that consist of 20 vertical and 14 horizontal segmented lines. When vertical and horizontal wires in the routing tracks cross each other, vias 202 are used to connect them.

[0022] FIG. 3 is an embodiment of the present invention showing a more detailed logic diagram of one of the cells of FIGs. 1 and 2. Logic cell 200 includes three look-up tables (LUT's), 302, 304 and 306, a flip-flop, 308, and two buffers or inverters, 310 and 312. LUT's X, 302, and Y, 304, each have three logic inputs A, B and C. LUT Z, 306, has two logic inputs A and B. The LUT inputs are shown at 301. The VDD and VSS signals are hard-wired into the logic cell 200 and are not shown. There is routing internal to the cell that allows any LUT to drive at least one input of any other LUT. The cell includes

two inverters, 310 and 312, that may also be buffers. The inverters or buffers serve to increase the drive strength of the output signals O1 and O2.

[0023] Logic cell 200 also includes flip-flop 308 that has an output Q and an input D that can be driven by any LUT. The CLK, RST, SE and SI signals are traditional scanned-flop clock, reset, scan-enable and scan-input that allow flip-flop 308 to be connected in a traditional scan chain for scan testing. The SE and SI signals are hard-wired into the cell. The exact clock scheme depends on the implementation, however there is a clock and reset signal generator every 8 rows of logic cells. These clock cells drive the reset and clock signals for the 8 logic cells directly below them. This allows flip-flop 308 within the cell 200 to be simplified, and enables testing by disabling all reset lines, and gating the test clock onto all flop clocks.

[0024] The configuration of the cell may be controlled in part by programming the via connections illustrated as 309. Jumpers J1, J2, J3 and J4 may provide for an increase in density by allowing some configuration of this portion of the cell outside of using the general purpose routing tracks. Signals R1, R2, R3 and R4 are wires that connect to the general purpose routing tracks that allow unbuffered signals to be routed short distances.

[0025] In a practical semiconductor device, each LUT may be provided with appropriate test data lines to send data from a selected column of the LUT to the edge of the chip die for testing. Of course, in such a case lines are also provided to determine which column's data is to be communicated to the edge

of the chip. FIGs. 3-5 illustrate an embodiment of a method and apparatus for testing a semiconductor device using the test read lines (TR) and test data lines (TD, TD1 and TD2). The signals TD1-TD3 in combination with TR1 and TR2 allow for up to 6 internal test points (3x2) of which 5 are used in one embodiment of the present invention. The test signals are hard-wired into the logic cell and are not routed using the general purpose routing tracks. In one embodiment of the present invention, read circuits are located at the end of each row of logic cells to read the data from the internal nodes of the LUT's by utilizing the test data lines. The internal nodes of the LUT's are read using a read circuit in such a manner that a significant charge is required in order to flip the state of the read line in the circuit which indicates that the internal nodes probed in the LUT are not floating. Previous test circuits would only check the output of the LUT's, which could be driven high or low with good strength even if the internal nodes were floating.

[0026] In one embodiment, a method of testing the device includes the use of test vectors that are generated in the traditional means (with an ATPG program). The test vectors are applied using a built-in scan-chain. While the results of a vector are valid, the internal LUT nodes are read onto the TD lines, one column at a time. A single column is enabled with a single TR line and then the TD lines send the values internal to the LUT's to the edge of the device where they can be processed. The read circuits at the edge of the die

may determine if the TD lines are being actively driven to a state, or if they are floating.

[0027] A LUT, as shown in FIG. 3, is built from one or more multiplexers with constant data inputs. The logic inputs into the cell drive the select lines of the multiplexers. A LUT of N inputs may be implemented with a multiplexer of 2^N data inputs programmably tied to one of the supply voltages through vias. FIG. 4 illustrates a 3-input LUT (similar to LUT's X and Y shown in FIG. 3) with a test circuit implemented in an 8-to-1 multiplexer as well as the method of using the test circuit. The logic inputs 402 drive the select lines of the multiplexer using the inverters 428, 430 and 432 that enable only one selected path through the multiplexer at a time. The data inputs 404 have constant inputs that are programmably tied to one of the supply voltages through vias. The LUT has two columns of n-channel mosfets 406 that are basically two 4-to-1 multiplexers. Notice that there are 8 pairs of n-channel mosfets in series. This could be implemented as 8 feeding 4; however, a better utilization of the layout area will occur with this implementation. The upper four pair of mosfets are enabled with the four possible combinations of A and not-A, and B and not-B. Depending on the state of the A and B select lines, one of these paths will be enabled, thus selecting a point that has been programmed to a logic 1 or 0. This is also true of the lower four pair of mosfets. The output circuitry 408 of the LUT implements a 2-to-1 multiplexer to select between the outputs of the two 4-to-1 multiplexers described above. The signals from the 4-to-1

multiplexers pass through inverters 410 and 412 to buffer and amplify the signals. Two weak p-channel mosfets 414 and 416 feed back around inverters 410 and 412 causing the inputs to inverters 410 and 412 to charge all the way to VDD when the data inputs are logic 1's. Otherwise, the data inputs would float at around VDD - Vth, thus potentially causing significant leakage through inverters 410 and 412. Two standard CMOS transition gates 418 and 420 are connected to the output of inverters 410 and 412 to select the output of either the upper 4-to-1 multiplexer, or the lower one, depending on the value of the C select line. The output signal of the LUT is driven out at a high strength by buffer 422. Finally, two transistors 424 and 426 are used for testing the LUT.

[0028] FIG. 5 illustrates a 2-input LUT (similar to LUT Z shown in FIG. 3) with a test circuit implemented in a 4-to-1 multiplexer as well as the method of using the test circuit. The logic inputs 502 drive the select lines of the multiplexer using the inverters 514 and 516 that enable only one selected path through the multiplexer at a time. The data inputs 504 have constant inputs that are programmably tied to one of the supply voltages through vias. The LUT has two columns of n-channel mosfets 506. Notice that there are 4 pairs of n-channel mosfets in series. The four pair of mosfets are enabled with the four possible combinations of A and not-A, and B and not-B. Depending on the state of the A and B select lines, one of these paths will be enabled, thus selecting a point that has been programmed to a logic 1 or 0. The signal from

the 4-to-1 multiplexer passes through inverter 508 to buffer and amplify the signal. A weak p-channel mosfet 510 is feed back around inverter 508 to cause the input to inverter 508 to charge all the way to VDD when the data inputs are logic 1's. Otherwise, the data inputs would float at around VDD - Vth, thus potentially causing significant leakage through inverter 508. Finally, transistor 512 is used for testing the LUT.

[0029] FIG. 6 illustrates an approximate, example layout of the logic elements in a cell on a chip like that discussed above with regard to FIG. 3. Programming vias are roughly located in a middle vertical strip in the logic cell; therefore, all of the LUT's need to be adjacent to these vias. The two 8-to-1 multiplexers 602 and 604 that implement the 3-input LUT's may be located in the upper half of the logic cell as shown with the data inputs aligned vertically just under the 32 programming vias located in the upper half of the cell. There are 8 more vias for the 4-to-1 multiplexer 606 that implements the 2-input LUT that may be placed on the left side of the logic cell. Flip-flop 608 is located on the right side of the cell because there is room available for it there. The two inverters 610 and 612 are used for extra drive strength and are shown at the bottom of the layout.

[0030] FIG. 7 illustrates the metal 4 (M4) and metal 5 (M5) layers of a typical ASIC using the invention with the M4 layer shown overlaying the M5 layer. The horizontal routing lines, 702, are illustrated in the upper half of FIG. 7 that jump to M5 in order to avoid the programming vias in the vertical lines,

704, located in middle section of the cell. The lower half of FIG. 7 illustrates M4 in the vertical direction, 706. There are vias, 708, to M3 in the upper end of the vertical M4 segments where the vertical lines, 706, continue to the next vertical segment above. In combination with the vias to M3, along the bottom of these vertical segments, we are able to break the vertical lines at the top, bottom, or middle of the cell. The jumpers J1, J2, J3 and J4, 710, (as shown in FIG. 3) can be seen in the lower portion of the vertical lines in the middle section of the cell. The VDD and VSS lines, 704, are located at the top of the cell for configuring the LUT's in the cell. In M5, notice the very wide vertical power strips 712 and 714 that should provide sufficient metal for excellent power distribution. C1 and C2, 716, are global clock lines in the vertical M5 metal that are used throughout the cell. Reset, test signal 1 and test signal 2 may also be routed in vertical M5 metal. The vertical line SE, 718, is scan-enable used in the flip-flop referred to in FIG. 3. In one embodiment of the invention, the vertical lines FH, FL and THD, 720, are free resources that may be used for routing signals in the cell, such as the test signals TR1 and TR2. The assignment of these resources depends on the exact layout used for the cell.

[0031] FIG. 8 illustrates the metal 3 (M3) and metal 4 (M4) layers with the M3 layer shown overlaying the M4 layer. In one embodiment, there are 20 vertical routing lines, 802, that span from the top of the cell to the bottom – these lines provide for the vertical general purpose routing. The vertical

routing lines 802 are in the M3 layer in the upper portion of the cell, and in the M4 layer in the lower portion of the cell. This allows horizontal I/O wires, 806 and 808, to cross them in the M3 layer in the lower portion of the cell. The labels shown in FIG. 8 are provided for convenience and correspond to the same labels shown in FIG. 3. There are 14 horizontal routing lines, 804, that span from the left to right of the cell, except as shown in FIG. 7 where the lines jump to the M5 layer in order to jump over the LUT programming and jumper vias shown in the middle strip of the cell.

[0032] FIG. 9 illustrates an embodiment of the metal 3 (M3) and metal 4 (M4) layers with the M4 layer shown overlaying the M3 layer and annotated with reference numbers to identify various groups of programming vias. Layout areas 901 allow the vertical routing lines on M3 to connect to the horizontal routing lines on M4. The left group of horizontal wires are shorted to the right group of horizontal wires through M5. The use of M5 jumps over the vias in groups 905 - 907. Layout areas 902 allow the LUT inputs, RST, CLK, and the outputs of the cell (R1 - R4, O1, O2) to connect to the vertical routing lines. There are four via groups, 903, that allow signals to travel from the lower portion of the vertical routing lines located on M4 layer of the cell to upper portion of the vertical routing lines located on the M3 layer of the cell. These vias 903 allow the vertical routing lines to be broken either at the bottom of the cell, or in the middle, or to connect to make longer wires. Four more groups of vias, 904, allow horizontal routing lines to be broken at the left

and right sides of the cell. There are 16 programming vias, 905, that are used to program one of the 3-input LUT's that is located below and to the left of these vias (see FIG. 6 for an example layout of the logic elements). There are 16 additional programming vias, 906, that are used to program the other 3-input LUT that is located below and to the right of these vias. There are eight programming vias, 907, that are used to program the 2-input LUT that is located somewhere below and possibly to the left of these vias. Vias 908 attach jumpers J1 – J4 to internal signals within the logic cell, which allows local connections to be made without using the general routing wires outside of the cell. Vias 909 connect the jumpers J1 – J4 to R1 – R4, and allows O1D and O2D to connect to the jumpers and VSS. O1D and O2D allow outputs O1 and O2 to either be driven directly, or to have one high-drive buffer, or to have both high-drive buffers in parallel. The horizontal section of vias, 910, allows four vertical signals on M4 to connect down to the metal 1 (M1) layer. This allows up to four test signals to be used. Horizontal VSS and VDD wires need to be routed on the metal 2 (M2) layer to form a grid with the vertical power wires on M5.

[0033] FIGs. 7-9 illustrate a method of making a semiconductor device utilizing the cell architecture shown in FIG. 3 according to at least some embodiments of the present invention. Initially, a semiconductor layer is formed which has a mask-configurable gate array with logic cells as shown in FIG 3. The logic cells in the semiconductor layer include at least two three-

input look-up tables, at least one two-input look-up table and a flip-flop. The look-up tables in the logic cells are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop. As illustrated in FIGs. 7-9, a plurality of metal layers are formed on top of the semiconductor layer for routing connections where at least some of the metal layers are used to configure the gate array logic cells.

[0034] The designs using an embodiment of the invention disclosed herein may be routed without having all of the via locations available to the router. This is not of much use if the vias are small enough to fit into the space occupied by the intersection of vertical and horizontal minimum width metal traces. However, if the via connections for some reason are larger than the metal pitch, it may be of great value to depopulate them. A 50% depopulation of the vias is preferable using some laser via technology that will provide almost twice the density and ensures that the programmable vias do not dominate the programming layer. Otherwise, a larger geometry via layer deposited over a small geometry wafer may work well with a similar architecture. Depending on the difference between the base wafer geometry and the top via and metal layer geometry, a depopulation of 0%-75% works well. For example, if the difference between metal pitch on lower layers of metal, and the top metal layer is 4x, a 75% depopulation scheme works well.

[0035] The embodiments of the invention as described herein may include the use of random access memory (RAM) that may be distributed throughout the logic array, so that a single cell fabric can provide both logic and RAM functionality. Additional information on the use of distributed RAM in a logic array can be found in the U.S. Patent application filed by William D. Cox with the United States Patent and Trademark Office on May 17, 2002, serial number 10/150,685, entitled "Distributed RAM in a Logic Array", which is incorporated herein by reference.

[0036] Specific embodiments of an invention are described herein. One of ordinary skill in the semiconductor arts will quickly recognize that the invention has other applications in other environments. In fact, many embodiments and implementations are possible. The following claims are in no way intended to limit the scope of the invention to the specific embodiments described above.

CLAIMS

I claim:

1. A semiconductor device comprising:

a plurality of logic cells interconnected using via connections between routing tracks that are disposed among a plurality of layers, wherein said logic cells comprise:

at least two three-input look-up tables;

at least one two-input look-up table;

a flip-flop; and

wherein the look-up tables are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

2. A semiconductor device according to claim 1 wherein the logic cells are programmable and the programming is determined using via connections between the routing tracks.

3. A semiconductor device according to claim 1 wherein at least one of said at least two three-input look-up tables comprises at least one multiplexer.

4. A semiconductor device according to claim 1 wherein said at least one two-input look-up table comprises at least one multiplexer.

5. A semiconductor device according to claim 1 wherein said logic cells further comprise at least one inverter to buffer and amplify an output signal of the logic cell.

6. A semiconductor device according to claim 1 wherein the logic cells are arranged in an array of programmable cells having a multiplicity of inputs and outputs.

7. A semiconductor device according to claim 1 wherein the device is an application specific integrated circuit.

8. A semiconductor device according to claim 2 wherein said logic cells are programmed for testing the logic functions of the cell during a testing process.

9. A semiconductor device according to claim 8 wherein the testing process comprises:

selecting at least one component in said logic cells to test;

sending test data to the at least one component; and

reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

10. A semiconductor device according to claim 1 wherein said plurality of layers includes at least three metal layers and a single custom via layer used to interconnect said components in said logic cells.

11. A method of making a semiconductor device, the method comprising:

forming a semiconductor layer comprising a mask-configurable gate array having logic cells that include at least two three-input look-up tables, at least one two-input look-up table and a flip-flop, wherein the look-up tables are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop; and

forming a plurality of metal layers disposed on top of the semiconductor layer for routing connections wherein at least some of the plurality of metal layers configures the gate array logic cells.

12. The method of claim 11 wherein the gate array logic cells are configured with only some of the plurality of metal layers.

13. The method of claim 11 wherein the gate array logic cells are substantially configured with only one of the plurality of metal layers.

14. The method of claim 13 wherein the one of the plurality of metal layers is a via layer.

15. A method of testing a programmable logic cell in a semiconductor device, the method comprising:

selecting at least one component in the logic cell to test;

sending test data to the at least one component; and

reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

16. The method of claim 15 wherein the at least one component is a look-up table.

17. The method of claim 16 wherein the look-up table comprises at least one multiplexer.

18. The method of claim 16 wherein the selecting step comprises selecting at least one column of the look-up table for testing.

19. The method of claim 15 wherein the sending step comprises generating test vectors and applying the test vectors using a built-in scan-chain.

20. The method of claim 15 wherein the reading step comprises sending data from the at least one component to the edge of the semiconductor device for testing.

21. A semiconductor device comprising apparatus for testing a programmable logic cell in the semiconductor device, wherein the apparatus comprises:

means for selecting at least one component in the logic cell to test;

means for sending test data to the at least one component; and

means for reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

22. A semiconductor device according to claim 21 wherein the at least one component is a look-up table.

23. A semiconductor device according to 22 wherein the look-up table comprises at least one multiplexer.

24. A semiconductor device according to claim 22 wherein the means for selecting comprises means for selecting at least one column of the look-up table for testing.

25. A semiconductor device according to claim 21 wherein the means for sending comprises means for generating test vectors and applying the test vectors using a built-in scan-chain.

26. A semiconductor device according to claim 21 wherein the means for reading comprises means for sending data from the at least one component to the edge of the semiconductor device for testing.

ABSTRACT OF THE DISCLOSURE

A semiconductor device and method of testing the device having a plurality of logic cells interconnected using vias to connect routing tracks that are disposed among a plurality of layers in the device. The logic cells in the device including at least two three-input look-up tables, one two-input look-up table and a flip-flop. The components in the logic cell are connected so that any look-up table can drive at least one input of any other look-up table and where the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

Reference AM

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Applicant(s)

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Domestic Priority data as claimed by applicant

THIS APPLN CLAIMS BENEFIT OF 60/296,854 06/08/2001

Foreign Applications

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**** SMALL ENTITY ****

Title

Cell architecture to reduce customization in a semiconductor device

CELL ARCHITECTURE TO REDUCE CUSTOMIZATION IN A SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from co-pending provisional patent application serial number 60/296,854, filed June 8, 2001, by the inventor hereof, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] For many years, gate arrays have been used to provide quick-turnaround, low non-recurring-expense (NRE) semiconductor devices that are used for a variety of purposes. Traditionally, semiconductor wafers are processed up to but not including the first (bottom) metal layer, and then the wafers are saved in inventory. When a customer orders a semiconductor device to be fabricated for a specific application (an application specific integrated circuit or "ASIC"), the customer only has to pay for the masks that are required to configure the metal layers, but not for the transistor layers below. Thus, NRE is reduced. The wafers may be completed quickly, since only the metal layers remain to be fabricated, which also reduces the turn-around time that is necessary to build the device.

[0003] Recently more and more layers of metal have been incorporated into gate array semiconductor devices. Rather than two or three layers of metal, six to eight layers of metal are now common. As a result, gate arrays

are no longer very low NRE, or provide quick-turnaround times. In order to regain the advantages of earlier gate arrays, several vendors have developed logic arrays, consisting of multiple, substantially identical logic cells, that may be configured for an application with either fewer or cheaper masks. In the case of fewer masks, the total number of metal layers and hence masks used to create the finished device often does not change. Rather, only a reduced subset of the total number of metal layers in a finished device are used to impart the custom configuration to the device. For example, so-called "one-mask" devices, in which only a single metal layer and hence a single mask imparts customization, may reduce both NRE and the turnaround-time.

[0004] An ASIC is a semiconductor device that combines large numbers of programmable blocks of logic circuits into a logic cell to create a device that is specifically adapted for a particular application, but at a cost that is lower than that of developing a completely new device from scratch. Like most integrated circuit chips, ASIC chips are manufactured using a lithographic process that depends on having a mask for each layer of the chip. In the case of a completely new chip, many unique masks may be required. In the case of an ASIC such as a gate array, however, some masks are generic, that is, the same for each different type of ASIC of a given programmable architecture, regardless of the application, while some are custom. It is the custom masks that impart the application specificity to the chip by programming the logic cells during the manufacturing process. Multiple custom masks may be required to

accomplish the programming of an ASIC. The number depends to some extent on the design of the programmable cells. Although the number of custom masks required is less than the total number of masks, and certainly less than the number of masks required to create a completely new chip from scratch, each custom mask represents a significant cost in both money and development time.

[0005] In many cases, the cell architecture of an ASIC may be designed to reduce the number of custom masks that may be required to just one mask, which provides a significant cost and time savings. A "one mask" device allows all of the masks to remain generic except for a single mask, thus allowing the semiconductor manufacturer to invest in the generic or base masks just one time. Various designs may be implemented by customizing just a single mask instead of a complete mask set.

SUMMARY

[0006] The present invention provides for a semiconductor device and a method of testing the device having a plurality of logic cells interconnected using vias to connect routing tracks that are disposed among a plurality of layers in the device. The logic cells in the device include at least two three-input look-up tables, one two-input look-up table and a flip-flop. The components in the logic cell are connected so that any look-up table can drive at least one input of any other look-up table and where the flip-flop is

connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

[0007] In some embodiments, the semiconductor device may be designed to be configured or customized using less than the actual number of metal (including via) layer masks that will actually be used to create a final device. In some cases, this configuration will be accomplished with a single metal layer mask, which may be either a mask designed to create a layer of actual metal traces, or a layer of vias which move signals between metal layers.

[0008] In any case, a completed device is made by first forming the semiconductor layer where cells contain mask-configurable gate array as described above. Then, the plurality of metal layers are formed on top of the semiconductor layer for routing connections. At least some of the plurality of metal layers are customized and may be used to configure the device for a specific application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 illustrates an 8 by 8 array of logic cells according to at least some embodiments of the present invention.

[0010] FIG. 2 illustrates a single logic cell and surrounding routing tracks according to the present invention.

[0011] FIG. 3 is a detailed logic diagram of a single cell architecture that may be used with the invention.

[0012] FIG. 4 illustrates an exemplary 3-input lookup table with a test circuit according to at least some embodiments of the present invention.

[0013] FIG. 5 illustrates an exemplary 2-input lookup table with a test circuit according to at least some embodiments of the present invention.

[0014] FIG. 6 illustrates an example layout of the logic elements of the cell shown in FIG. 3.

[0015] FIG. 7 illustrates the metal 4 and 5 layers of a typical ASIC using the present invention.

[0016] FIG. 8 illustrates the metal 3 and 4 layers of a typical ASIC using the present invention.

[0017] FIG. 9 illustrates the metal 3 and 4 layers of a typical ASIC with annotations to identify groups of programming vias according to at least some embodiments of the present invention.

DESCRIPTION OF THE INVENTION

[0018] It is to be understood that the present invention is not limited to the example embodiments disclosed herein. The meaning of certain terms as used in the context of this disclosure should be understood as follows. The term "configuration" and variants such as "configurable" and "configured" refer to the property or process of imparting application-specific function to an integrated circuit chip. The term "metal layer" refers to any layers that are used to make connections to implement the functions of the cells of a device.

These metal layers may be the same for every version of a semiconductor device, or they may be used for configuration. In addition, metal layers may contain actual metal routing traces or vias, which provide vertical connectivity between metal routing layers. Finally, the term "chip" and variations such as "integrated circuit chip" or "semiconductor chip" are normally meant to refer to an intermediate device that has not been configured, and may be in the form of a wafer. A finished device such as an application-specific integrated circuit (ASIC) will be referred to as a "device" or with a variant term such as "semiconductor device" or the like. Other terms will either be discussed when introduced, or otherwise should be assumed to have the conventional meaning as understood by persons of ordinary skill in the art.

[0019] The present invention in some embodiments defines a cell architecture for an ASIC that reduces the number of custom masks required to just one mask, representing significant cost and time savings. In some embodiments, the invention allows all of the masks to remain generic except for the via mask, which determines where the so-called "vias" will be placed to make connections between layers. By using the architecture of the invention, the semiconductor manufacturer may invest in the generic or base masks just one time. Various designs are then implemented by customizing just the via mask instead of a complete mask set.

[0020] A device according to the present invention has rows and columns of logic cells, where each cell may implement about 10 ASIC gates worth of

logic. FIG. 1 illustrates an 8 by 8 array of logic cells 100 that would have 32 pads 102 around the edge of the die. Horizontal routing tracks 104 and vertical routing tracks 106 connect the logic cells 100 together. These tracks are formed of segmented wires of fixed length that may be connected end-to-end through vias, which are shown in more detail in FIG. 2. The inputs and outputs of the logic cells 100 communicate using routing tracks 104 and 106 through the vias.

[0021] FIG. 2 illustrates a single logic cell 200 and how the cell connects to surrounding cells. The logic cell 200 is connected to the other logic cells in the array using the horizontal and vertical routing tracks 104 and 106 that consist of 20 vertical and 14 horizontal segmented lines. When vertical and horizontal wires in the routing tracks cross each other, vias 202 are used to connect them.

[0022] FIG. 3 is an embodiment of the present invention showing a more detailed logic diagram of one of the cells of FIGs. 1 and 2. Logic cell 200 includes three look-up tables (LUT's), 302, 304 and 306, a flip-flop, 308, and two buffers or inverters, 310 and 312. LUT's X, 302, and Y, 304, each have three logic inputs A, B and C. LUT Z, 306, has two logic inputs A and B. The LUT inputs are shown at 301. The VDD and VSS signals are hard-wired into the logic cell 200 and are not shown. There is routing internal to the cell that allows any LUT to drive at least one input of any other LUT. The cell includes

two inverters, 310 and 312, that may also be buffers. The inverters or buffers serve to increase the drive strength of the output signals O1 and O2.

[0023] Logic cell 200 also includes flip-flop 308 that has an output Q and an input D that can be driven by any LUT. The CLK, RST, SE and SI signals are traditional scanned-flop clock, reset, scan-enable and scan-input that allow flip-flop 308 to be connected in a traditional scan chain for scan testing. The SE and SI signals are hard-wired into the cell. The exact clock scheme depends on the implementation, however there is a clock and reset signal generator every 8 rows of logic cells. These clock cells drive the reset and clock signals for the 8 logic cells directly below them. This allows flip-flop 308 within the cell 200 to be simplified, and enables testing by disabling all reset lines, and gating the test clock onto all flop clocks.

[0024] The configuration of the cell may be controlled in part by programming the via connections illustrated as 309. Jumpers J1, J2, J3 and J4 may provide for an increase in density by allowing some configuration of this portion of the cell outside of using the general purpose routing tracks. Signals R1, R2, R3 and R4 are wires that connect to the general purpose routing tracks that allow unbuffered signals to be routed short distances.

[0025] In a practical semiconductor device, each LUT may be provided with appropriate test data lines to send data from a selected column of the LUT to the edge of the chip die for testing. Of course, in such a case lines are also provided to determine which column's data is to be communicated to the edge

of the chip. FIGs. 3-5 illustrate an embodiment of a method and apparatus for testing a semiconductor device using the test read lines (TR) and test data lines (TD, TD1 and TD2). The signals TD1-TD3 in combination with TR1 and TR2 allow for up to 6 internal test points (3x2) of which 5 are used in one embodiment of the present invention. The test signals are hard-wired into the logic cell and are not routed using the general purpose routing tracks. In one embodiment of the present invention, read circuits are located at the end of each row of logic cells to read the data from the internal nodes of the LUT's by utilizing the test data lines. The internal nodes of the LUT's are read using a read circuit in such a manner that a significant charge is required in order to flip the state of the read line in the circuit which indicates that the internal nodes probed in the LUT are not floating. Previous test circuits would only check the output of the LUT's, which could be driven high or low with good strength even if the internal nodes were floating.

[0026] In one embodiment, a method of testing the device includes the use of test vectors that are generated in the traditional means (with an ATPG program). The test vectors are applied using a built-in scan-chain. While the results of a vector are valid, the internal LUT nodes are read onto the TD lines, one column at a time. A single column is enabled with a single TR line and then the TD lines send the values internal to the LUT's to the edge of the device where they can be processed. The read circuits at the edge of the die

may determine if the TD lines are being actively driven to a state, or if they are floating.

[0027] A LUT, as shown in FIG. 3, is built from one or more multiplexers with constant data inputs. The logic inputs into the cell drive the select lines of the multiplexers. A LUT of N inputs may be implemented with a multiplexer of 2^N data inputs programmably tied to one of the supply voltages through vias. FIG. 4 illustrates a 3-input LUT (similar to LUT's X and Y shown in FIG. 3) with a test circuit implemented in an 8-to-1 multiplexer as well as the method of using the test circuit. The logic inputs 402 drive the select lines of the multiplexer using the inverters 428, 430 and 432 that enable only one selected path through the multiplexer at a time. The data inputs 404 have constant inputs that are programmably tied to one of the supply voltages through vias. The LUT has two columns of n-channel mosfets 406 that are basically two 4-to-1 multiplexers. Notice that there are 8 pairs of n-channel mosfets in series. This could be implemented as 8 feeding 4; however, a better utilization of the layout area will occur with this implementation. The upper four pair of mosfets are enabled with the four possible combinations of A and not-A, and B and not-B. Depending on the state of the A and B select lines, one of these paths will be enabled, thus selecting a point that has been programmed to a logic 1 or 0. This is also true of the lower four pair of mosfets. The output circuitry 408 of the LUT implements a 2-to-1 multiplexer to select between the outputs of the two 4-to-1 multiplexers described above. The signals from the 4-to-1

multiplexers pass through inverters 410 and 412 to buffer and amplify the signals. Two weak p-channel mosfets 414 and 416 feed back around inverters 410 and 412 causing the inputs to inverters 410 and 412 to charge all the way to VDD when the data inputs are logic 1's. Otherwise, the data inputs would float at around VDD - Vth, thus potentially causing significant leakage through inverters 410 and 412. Two standard CMOS transition gates 418 and 420 are connected to the output of inverters 410 and 412 to select the output of either the upper 4-to-1 multiplexer, or the lower one, depending on the value of the C select line. The output signal of the LUT is driven out at a high strength by buffer 422. Finally, two transistors 424 and 426 are used for testing the LUT.

[0028] FIG. 5 illustrates a 2-input LUT (similar to LUT Z shown in FIG. 3) with a test circuit implemented in a 4-to-1 multiplexer as well as the method of using the test circuit. The logic inputs 502 drive the select lines of the multiplexer using the inverters 514 and 516 that enable only one selected path through the multiplexer at a time. The data inputs 504 have constant inputs that are programmably tied to one of the supply voltages through vias. The LUT has two columns of n-channel mosfets 506. Notice that there are 4 pairs of n-channel mosfets in series. The four pair of mosfets are enabled with the four possible combinations of A and not-A, and B and not-B. Depending on the state of the A and B select lines, one of these paths will be enabled, thus selecting a point that has been programmed to a logic 1 or 0. The signal from

the 4-to-1 multiplexer passes through inverter 508 to buffer and amplify the signal. A weak p-channel mosfet 510 is feed back around inverter 508 to cause the input to inverter 508 to charge all the way to VDD when the data inputs are logic 1's. Otherwise, the data inputs would float at around VDD - Vth, thus potentially causing significant leakage through inverter 508. Finally, transistor 512 is used for testing the LUT.

[0029] FIG. 6 illustrates an approximate, example layout of the logic elements in a cell on a chip like that discussed above with regard to FIG. 3. Programming vias are roughly located in a middle vertical strip in the logic cell; therefore, all of the LUT's need to be adjacent to these vias. The two 8-to-1 multiplexers 602 and 604 that implement the 3-input LUT's may be located in the upper half of the logic cell as shown with the data inputs aligned vertically just under the 32 programming vias located in the upper half of the cell. There are 8 more vias for the 4-to-1 multiplexer 606 that implements the 2-input LUT that may be placed on the left side of the logic cell. Flip-flop 608 is located on the right side of the cell because there is room available for it there. The two inverters 610 and 612 are used for extra drive strength and are shown at the bottom of the layout.

[0030] FIG. 7 illustrates the metal 4 (M4) and metal 5 (M5) layers of a typical ASIC using the invention with the M4 layer shown overlaying the M5 layer. The horizontal routing lines, 702, are illustrated in the upper half of FIG. 7 that jump to M5 in order to avoid the programming vias in the vertical lines,

704, located in middle section of the cell. The lower half of FIG. 7 illustrates M4 in the vertical direction, 706. There are vias, 708, to M3 in the upper end of the vertical M4 segments where the vertical lines, 706, continue to the next vertical segment above. In combination with the vias to M3, along the bottom of these vertical segments, we are able to break the vertical lines at the top, bottom, or middle of the cell. The jumpers J1, J2, J3 and J4, 710, (as shown in FIG. 3) can be seen in the lower portion of the vertical lines in the middle section of the cell. The VDD and VSS lines, 704, are located at the top of the cell for configuring the LUT's in the cell. In M5, notice the very wide vertical power strips 712 and 714 that should provide sufficient metal for excellent power distribution. C1 and C2, 716, are global clock lines in the vertical M5 metal that are used throughout the cell. Reset, test signal 1 and test signal 2 may also be routed in vertical M5 metal. The vertical line SE, 718, is scan-enable used in the flip-flop referred to in FIG. 3. In one embodiment of the invention, the vertical lines FH, FL and THD, 720, are free resources that may be used for routing signals in the cell, such as the test signals TR1 and TR2. The assignment of these resources depends on the exact layout used for the cell.

[0031] FIG. 8 illustrates the metal 3 (M3) and metal 4 (M4) layers with the M3 layer shown overlaying the M4 layer. In one embodiment, there are 20 vertical routing lines, 802, that span from the top of the cell to the bottom – these lines provide for the vertical general purpose routing. The vertical

routing lines 802 are in the M3 layer in the upper portion of the cell, and in the M4 layer in the lower portion of the cell. This allows horizontal I/O wires, 806 and 808, to cross them in the M3 layer in the lower portion of the cell. The labels shown in FIG. 8 are provided for convenience and correspond to the same labels shown in FIG. 3. There are 14 horizontal routing lines, 804, that span from the left to right of the cell, except as shown in FIG. 7 where the lines jump to the M5 layer in order to jump over the LUT programming and jumper vias shown in the middle strip of the cell.

[0032] FIG. 9 illustrates an embodiment of the metal 3 (M3) and metal 4 (M4) layers with the M4 layer shown overlaying the M3 layer and annotated with reference numbers to identify various groups of programming vias. Layout areas 901 allow the vertical routing lines on M3 to connect to the horizontal routing lines on M4. The left group of horizontal wires are shorted to the right group of horizontal wires through M5. The use of M5 jumps over the vias in groups 905 - 907. Layout areas 902 allow the LUT inputs, RST, CLK, and the outputs of the cell (R1 - R4, O1, O2) to connect to the vertical routing lines. There are four via groups, 903, that allow signals to travel from the lower portion of the vertical routing lines located on M4 layer of the cell to upper portion of the vertical routing lines located on the M3 layer of the cell. These vias 903 allow the vertical routing lines to be broken either at the bottom of the cell, or in the middle, or to connect to make longer wires. Four more groups of vias, 904, allow horizontal routing lines to be broken at the left

and right sides of the cell. There are 16 programming vias, 905, that are used to program one of the 3-input LUT's that is located below and to the left of these vias (see FIG. 6 for an example layout of the logic elements). There are 16 additional programming vias, 906, that are used to program the other 3-input LUT that is located below and to the right of these vias. There are eight programming vias, 907, that are used to program the 2-input LUT that is located somewhere below and possibly to the left of these vias. Vias 908 attach jumpers J1 – J4 to internal signals within the logic cell, which allows local connections to be made without using the general routing wires outside of the cell. Vias 909 connect the jumpers J1 – J4 to R1 – R4, and allows O1D and O2D to connect to the jumpers and VSS. O1D and O2D allow outputs O1 and O2 to either be driven directly, or to have one high-drive buffer, or to have both high-drive buffers in parallel. The horizontal section of vias, 910, allows four vertical signals on M4 to connect down to the metal 1 (M1) layer. This allows up to four test signals to be used. Horizontal VSS and VDD wires need to be routed on the metal 2 (M2) layer to form a grid with the vertical power wires on M5.

[0033] FIGs. 7-9 illustrate a method of making a semiconductor device utilizing the cell architecture shown in FIG. 3 according to at least some embodiments of the present invention. Initially, a semiconductor layer is formed which has a mask-configurable gate array with logic cells as shown in FIG 3. The logic cells in the semiconductor layer include at least two three-

input look-up tables, at least one two-input look-up table and a flip-flop. The look-up tables in the logic cells are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop. As illustrated in FIGs. 7-9, a plurality of metal layers are formed on top of the semiconductor layer for routing connections where at least some of the metal layers are used to configure the gate array logic cells.

[0034] The designs using an embodiment of the invention disclosed herein may be routed without having all of the via locations available to the router. This is not of much use if the vias are small enough to fit into the space occupied by the intersection of vertical and horizontal minimum width metal traces. However, if the via connections for some reason are larger than the metal pitch, it may be of great value to depopulate them. A 50% depopulation of the vias is preferable using some laser via technology that will provide almost twice the density and ensures that the programmable vias do not dominate the programming layer. Otherwise, a larger geometry via layer deposited over a small geometry wafer may work well with a similar architecture. Depending on the difference between the base wafer geometry and the top via and metal layer geometry, a depopulation of 0%-75% works well. For example, if the difference between metal pitch on lower layers of metal, and the top metal layer is 4x, a 75% depopulation scheme works well.

[0035] The embodiments of the invention as described herein may include the use of random access memory (RAM) that may be distributed throughout the logic array, so that a single cell fabric can provide both logic and RAM functionality. Additional information on the use of distributed RAM in a logic array can be found in the U.S. Patent application filed by William D. Cox with the United States Patent and Trademark Office on May 17, 2002, serial number 10/150,685, entitled "Distributed RAM in a Logic Array", which is incorporated herein by reference.

[0036] Specific embodiments of an invention are described herein. One of ordinary skill in the semiconductor arts will quickly recognize that the invention has other applications in other environments. In fact, many embodiments and implementations are possible. The following claims are in no way intended to limit the scope of the invention to the specific embodiments described above.

CLAIMS

I claim:

1. A semiconductor device comprising:

a plurality of logic cells interconnected using via connections between routing tracks that are disposed among a plurality of layers, wherein said logic cells comprise:

at least two three-input look-up tables;

at least one two-input look-up table;

a flip-flop; and

wherein the look-up tables are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

2. A semiconductor device according to claim 1 wherein the logic cells are programmable and the programming is determined using via connections between the routing tracks.

3. A semiconductor device according to claim 1 wherein at least one of said at least two three-input look-up tables comprises at least one multiplexer.

4. A semiconductor device according to claim 1 wherein said at least one two-input look-up table comprises at least one multiplexer.

5. A semiconductor device according to claim 1 wherein said logic cells further comprise at least one inverter to buffer and amplify an output signal of the logic cell.

6. A semiconductor device according to claim 1 wherein the logic cells are arranged in an array of programmable cells having a multiplicity of inputs and outputs.

7. A semiconductor device according to claim 1 wherein the device is an application specific integrated circuit.

8. A semiconductor device according to claim 2 wherein said logic cells are programmed for testing the logic functions of the cell during a testing process.

9. A semiconductor device according to claim 8 wherein the testing process comprises:

selecting at least one component in said logic cells to test;

sending test data to the at least one component; and

reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

10. A semiconductor device according to claim 1 wherein said plurality of layers includes at least three metal layers and a single custom via layer used to interconnect said components in said logic cells.

11. A method of making a semiconductor device, the method comprising:

forming a semiconductor layer comprising a mask-configurable gate array having logic cells that include at least two three-input look-up tables, at least one two-input look-up table and a flip-flop, wherein the look-up tables are interconnected so that any one look-up table can drive at least one input of at least one other look-up table and the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop; and

forming a plurality of metal layers disposed on top of the semiconductor layer for routing connections wherein at least some of the plurality of metal layers configures the gate array logic cells.

12. The method of claim 11 wherein the gate array logic cells are configured with only some of the plurality of metal layers.

13. The method of claim 11 wherein the gate array logic cells are substantially configured with only one of the plurality of metal layers.

14. The method of claim 13 wherein the one of the plurality of metal layers is a via layer.

15. A method of testing a programmable logic cell in a semiconductor device, the method comprising:

selecting at least one component in the logic cell to test;

sending test data to the at least one component; and

reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

16. The method of claim 15 wherein the at least one component is a look-up table.

17. The method of claim 16 wherein the look-up table comprises at least one multiplexer.

18. The method of claim 16 wherein the selecting step comprises selecting at least one column of the look-up table for testing.

19. The method of claim 15 wherein the sending step comprises generating test vectors and applying the test vectors using a built-in scan-chain.

20. The method of claim 15 wherein the reading step comprises sending data from the at least one component to the edge of the semiconductor device for testing.

21. A semiconductor device comprising apparatus for testing a programmable logic cell in the semiconductor device, wherein the apparatus comprises:

means for selecting at least one component in the logic cell to test;

means for sending test data to the at least one component; and

means for reading the internal nodes of the at least one component using a read circuit in such a manner so as to require a significant charge to flip the state of a read line in the read circuit to indicate that the internal nodes of the at least one component are not floating.

22. A semiconductor device according to claim 21 wherein the at least one component is a look-up table.

23. A semiconductor device according to 22 wherein the look-up table comprises at least one multiplexer.

24. A semiconductor device according to claim 22 wherein the means for selecting comprises means for selecting at least one column of the look-up table for testing.

25. A semiconductor device according to claim 21 wherein the means for sending comprises means for generating test vectors and applying the test vectors using a built-in scan-chain.

26. A semiconductor device according to claim 21 wherein the means for reading comprises means for sending data from the at least one component to the edge of the semiconductor device for testing.

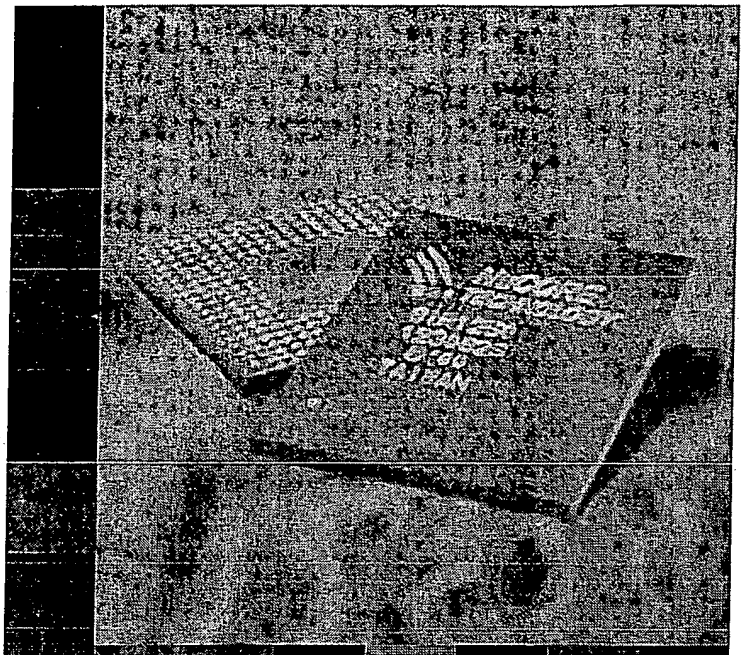
ABSTRACT OF THE DISCLOSURE

A semiconductor device and method of testing the device having a plurality of logic cells interconnected using vias to connect routing tracks that are disposed among a plurality of layers in the device. The logic cells in the device including at least two three-input look-up tables, one two-input look-up table and a flip-flop. The components in the logic cell are connected so that any look-up table can drive at least one input of any other look-up table and where the flip-flop is connected to the look-up tables so that any look-up table can drive an input of the flip-flop.

Reference AO 2 pages

NuCORE TECHNOLOGY

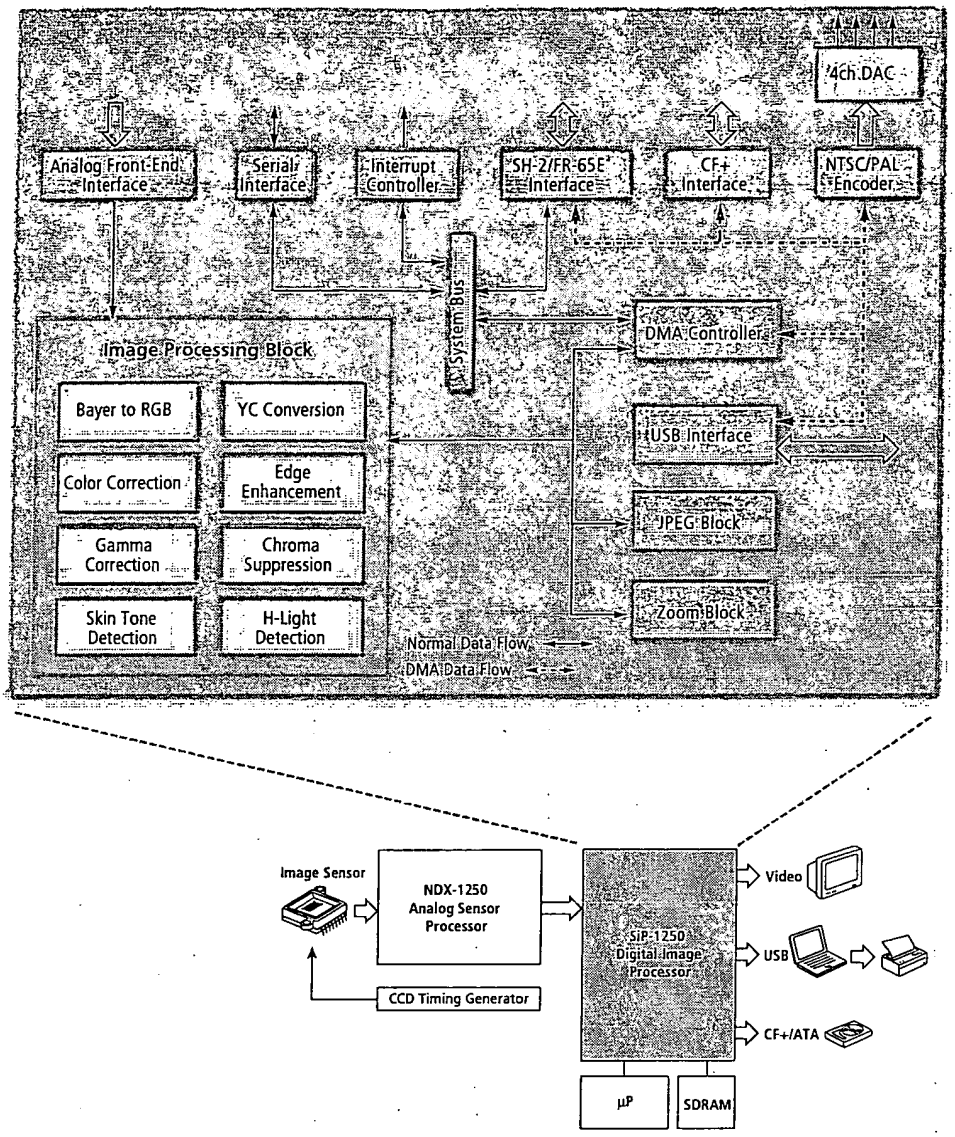
SiP-1250
Smart Image Processor



NuCORE's SiP-1250 is a high-performance digital image processor that when combined with NuCORE's companion chip, the NDX-1250 Sensor Processor and a CCD or CMOS image sensor, offers a complete image processing solution for digital cameras with resolutions up to 4 megapixels. The SiP-1250 integrates image processing blocks, a DMA controller, video encoding with line drivers and several standard memory and data interfaces (CF+, SDRAM, USB, Serial, Hitachi SH-2, Fujitsu FR-65E) into a single high-density package.

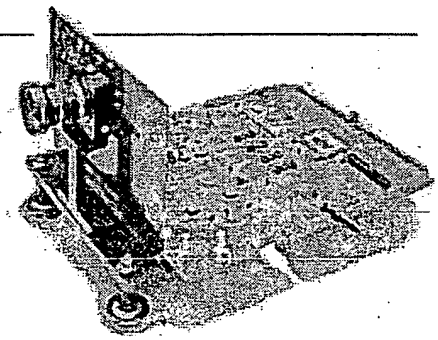
Operating at speeds up to 50 megapixels per second, the SiP-1250 is the world's fastest image processor for digital cameras and camcorders, providing fast, high-quality video and still image capture.

FEATURES	BENEFITS
Patented SiP Technology™ (Smart Image Processing)	Film quality still images for display and printing
Hardware JPEG codec	Realtime video rate compression up to 30 frames/sec
Highly optimized pipe-lined image processing architecture	Up to 50 megapixel/sec image data throughput enables hybrid still and video camera
50 MHz 12-bit interface to analog front-end processor	Offers easily tuned camera system without performance loss
Programmable zoom engine and resizer	Supports variety of view finder and capture modes
Bad pixel compensation corrects CCD errors	Improves image quality
On-chip NTSC/PAL encoders & USB, CF+, µP interfaces	Improves battery life while maintaining performance
Very low power consumption — less than 500mW at full speed	System-on-chip reduces part count and costs
Efficient memory architecture with on-chip memory	Reduced footprint and system cost with minimum amount of camera memory
High density Packaging - 280 FPBGA (0.8 mm ball pitch)	Reduced form factor



The SiP-1250 can interface with most Analog Front End (AFE) chips for digital camera applications. The figure above shows a system level implementation of a digital camera using NDX-1250 Sensor Processor and NuCORE's SiP-1250 Image Processor chips.

NuCORE Development Kit



The NuCORE Development Kit (NDK) includes a SiP-1250 based digital still camera, microprocessor board, software tools, and PC drivers — making it a complete reference design platform and prototyping tool. The modular design allows OEMs to develop and test different hardware and software components as part of their development cycle.

The NDK includes:

- *NDX-1250 Sensor Processor board with CCD Sensor-Lens*
- *SiP-1250 Digital Processor board with memory and peripherals*
- *Microprocessor Board (SH2)*
- *Software Modules (tools to compile, assemble, link, and execute code)*

Applications

- Digital Still Cameras
- Digital Video Camcorders
- PDA Cameras
- Machine Vision Applications
- Medical Imager
- Security Cameras

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